ESD Protection of an RF Integrated Circuit by Embedding Protection in the IC Package Printed Circuit Board

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I. Introduction

With the trend towards smaller semiconductor chip geometries, higher frequencies, and the escalating number of signal lines, damage of electronic products from electrostatic discharge (ESD) has increased due to the shear number of signal lines and increasingly sensitive components. At the same time both the space and the capacitance budgets circuit designers allow for a product's ESD protection are decreasing. The capacitance of a protection component is a critical characteristic because too much capacitance degrades high speed digital signals. The capacitance requirements for GHz signals are 100's of fF as compared to 1000's of fF for MHz signals. This change in capacitance requirements has created a roadblock for use of traditional ESD protection components. Polymer Voltage Suppressors (PVS) are a new technology for ESD suppression that has the needed low capacitance for today's high frequency products. As signal lead count increases, the amount of real estate needed for ESD protection on semiconductors input/outputs (IOs) and on PCB IOs increases, making PVS ESD protection embedded in a PCB increasingly desirable . [1]

The higher number of passive components needed for high density, high frequency IC's , has led to continuous shrinking of passive components size, increased use of passive component arrays, and an increasing trend to embedding passive resistors and capacitors in the PCB. Embedding ESD protection in the IC package or the printed circuit board (PCB) is a logical approach to ESD protection that has numerous benefits.

By embedding ESD protection as a layer in the package of an IC PCB, the ESD protection is in close proximity all of the IC signal lines. The simultaneous protection of all signal lines allows protection not only shunting ESD from signal line to ground, but also by shunting ESD that occurs between signal lines to ground for total ESD protection. Figure 1 shows Electronic Polymers Inc. embedded EPI-CORE™ in a 4 layer printed circuit board of a RF module.

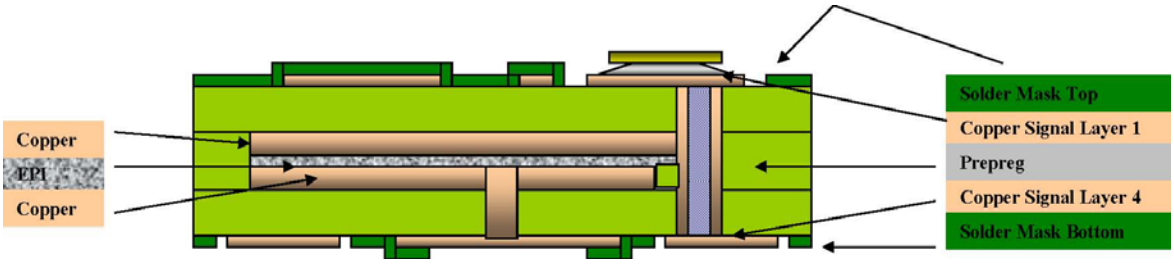

Figure 1 Fabrication Design for embedded EPI-CORE™ ESD protection layer in a 4 layer RF module.

The EPI-CORE™ consists of a PVS film, EPI-FLO™, that is coated on PCB copper panels and then laminated to give a copper/EPI-FLO™/copper core for a printed circuit board. Using printed circuit board manufacturing processes, the EPI-CORE™ is imaged and etched to produce the electrode pattern needed to tie the PVS ESD protection layer to signal vias and the ground plane. Once the EPI-CORE™ is etched, it is then laminated between FR-4 prepreg. Subsequent processing of the board uses typical printed circuit board manufacturing equipment.

Embedding ESD protection in the board is aligned with the National Electronics Manufacturing Technology Roadmap (NEMI) focus to reduce the number of passive components on the PCB by embedding passives in the PCB. The NEMI roadmap forecasts 40% penetration of embedded passives into the PCB market by 2008. [2]. Embedding EPI-CORE™ Polymer Voltage Suppressors Cores in a PCB is an enabling product for GaAs IC's that do not have ESD protection on the IC. Embedded PVS cores can be used for multiple pin protection and protection between the various pin combinations tested by HBM and MM ESD standards, minimizing on chip ESD requirements. The overcall cost benefits of replacing passive components with embedded components is well documented. Process steps for placing a passive component are eliminated, as is the board space utilized by the passive component.

To provide ESD protection of RF electronic products, EPI-FLO™ PVS surface mount devices and connector arrays were designed with low femto farad capacitance, low profile, (less than 10 mils) and multiple line ESD protection. The EPI-FLO™ polymer has an inherently low dielectric constant compared to the silicon diodes traditionally used for ESD protection. Typical surface mount devices are less than 200 fF. The progression from a surface mount EPI-FLO™ with single line ESD protection to multiple line ESD protection using USB and RJ-45 connector arrays lead to the design for embedded EPI-FLO™ cores.

It has been shown that the laminate used for EPI-FLO™ PVS connector arrays is suitable for direct embedding in PCB. The PVS connector arrays provide multiple line ESD protection without using PCB space. Figures 2 shows the multiple device EPI-FLO™ connector array and Figure 3 shows the laminate construction of the EPI-FLO™ Surface Mount device. [3]

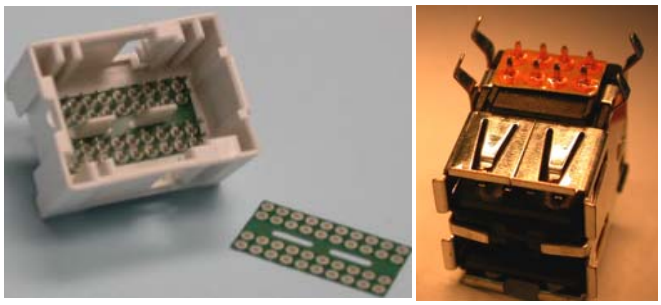

Figure 2. ESD Connector Array on 40 pin MQS automotive engine control module connector.

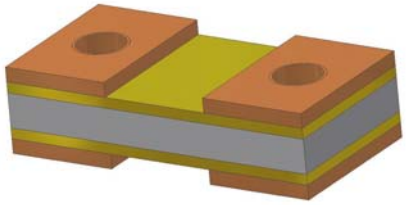

Figure 3. PVS Construction for 0603, 0402, 0201 Surface Mount Device

The PVS works by shunting ESD pulse to ground in nanoseconds. In the case of the connector array isolated copper washers are in contact with signal pins, and separated from the copper ground plane by the voltage sensing EPI-FLO™ polymer film. During an ESD event the EPI-FLO™ switches from high resistance to low resistance in nanoseconds, shunting the ESD pulse from the pin through EPI-FLO™ to ground through the ground pin on the connector. Manufacture of EPI-FLO™ connector arrays and the surface mount devices uses processes similar to PCB manufacturing processes allowing 1000's of devices to be made per industry standard 18"x24" board.

Establishing EPI-FLO™ PVS device specifications for protecting IC's led to the development of Transmission Line Pulse (TLP) test equipment and ESD procedures for correlation of PVS device trigger voltage performance to MM (Machine Model), HBM (Human Body Model) and IEC 61000-4-2 (System Level) ESD standards [4]. To use PVS devices for component level ESD conformance we developed test procedures and equipment to measure the ESD gun and TLP input voltage that causes a RF component to fail when powered post ESD pulsing. By correlating PVS device TLP pulse endurance (6-20 pulses) to the ESD specification required, and then selecting a lower TLP trigger voltage for the EPI-FLO™ than the device under test (DUT) TLP damage voltage a protection trigger voltage is determined. Using this protocol a PVS device can be specified to allow GaAs components that fail HBM and MM ESD without protection to be ESD compliant through the use of EPI-FLO™ devices.

The test procedures developed combine testing practices used for design of HBM on chip ESD protection [5-6] with TLP test methods that correlate to the pulse delivered by ESD Standard equipment.

II. System RF/ESD Compliance Procedure and Equipment

Test measurements are performed using a 50 ohm TLP system, an HBM ESD gun and HBM IC tester, and a MM ESD gun and MM IC tester. RF performance of a power amplifier module with and without a low capacitance 0603 surface mount EPI-FLO™ ESD protection component was measured at time zero and after ESD failure. The first step was to characterize the GaAs power amplifier modules for RF performance and for the I-V performance on a curve tracer from 0 to 2.5V prior to ESD or TLP testing. The module to be protected had 6 pins with 21 possible test combinations. The current was recorded at 1.5V and a 20% change in the current was set as device failure. ESD zapping was HBM and MM, 1 time per voltage, with 1 positive and 1 negative pulse. The current at 1.5V was measured before and after zapping for comparison. RF measurements were taken after devices failed the I-V criterion of no greater than 20% change in current.

The TLP test procedure is 5 pulses positive and 5 pulses negative. Traces were recorded after 3+, and 3− pulses, and leakage current at 1.5 V was recorded after each pulse. Testing was stopped after device failure increased from μA to mA. The 21 pin combinations were tested at 25 volt increments, then the most sensitive combinations were selected for retest and the step increments were fine tuned to 10 V to see the critical TLP damage level. Next EPI-FLO™ 0603 devices with trigger voltages less than the GaAs pin damage threshold were soldered on the test board. ESD testing using the HBM

ESD standard showed the GaAs survived HBM testing with an 80Vtrigger voltage EPI-FLO™ protection.

III. Correlation of TLP Test Data for GaAs Power Amplifier Modules with Integrated PVS Protection

Incorporation of an 80 Volt PVS 0603 surface mount device on the most sensitive pin combination, Vcontrol/Vground, increased ESD survival from 1 pulse of 450V HBM to >10 1000V HBM pulses. The least sensitive pins survived tens of pulses at 2000 V HBM.

As shown in Figure 4 the GaAs power amplifier failed at 450V and exhibited sudden death phenomena in that the leakage current increased from µA to mA. With PVS ESD protection the GaAs power amplifier module leakage current increase was a few µA with each pulse, not mA.

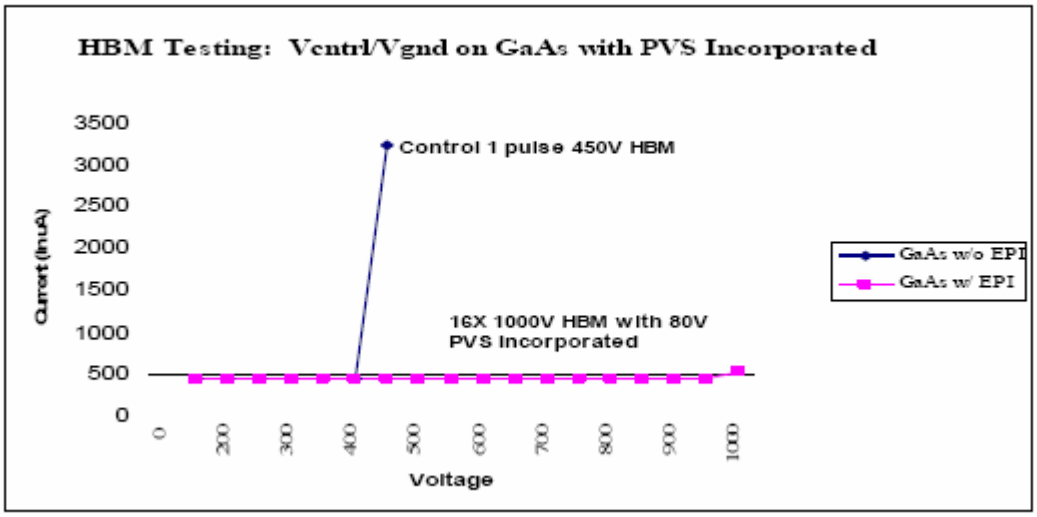

Figure 4: HBM ESD survivability of GaAs IC increases from 450 to 1000 V with 80V trigger EPI-FLO™ surface mount device.

IV. Summary

Since EPI-FLO™ connector arrays are manufactured in industry standard 12”x18” panels their manufacture is readily adaptable to an embedded layer in a PCB. To minimize size the overall dimensions of the copper-EPI-FLO™ laminate is held to 3 mils. Cost is based on a panel basis for ESD protection across the entire panel. For protection of RF power module an 80Vtrigger laminate is required.

Currently, mechanical verification of an embedded EPI-CORE™ in a 4 layer board has been completed. Next steps include electrical verification of ESD performance of a fully embedded device and design rule development for artwork. Manufacturing readiness is

running concurrently and is based on completion of qualification tests for a packaged GaAs IC. The initial target market is the RF module market since the ESD susceptibility is high, yet the demand for these high performance IC's is also high.

Since EPI-FLO™ has demonstrated ESD protection of GaAs it is contemplated that in the future, PVS films can replace the current usage of on-chip protection, opening up new markets, obtaining improved ESD protection for GaAs, and the for the 100 to 200 GHz Silicon Germanium heterojunction bipolar technologies. [7] It is also contemplated that EPI-CORE™ embedded in IC packages and in PCB eliminates roadblocks to continuous evolution of Moore's Law.

References

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[7] K. Shrier, T. Truong, and J. Felps, "Transmission Line Pulse Test Methods, Test Techniques and Characterization of Low Capacitance Voltage Suppression Device for System Level Electrostatic Discharge Compliance," ESDA Symposium, 2005.