

Transmission Line Pulse Methods, Test Techniques and Characterization of Low Capacitance Voltage Suppression Device for System Level Electrostatic Discharge Compliance

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Outline

- Motivation and Purpose
- System Versus Chip ESD
- The ESD Standards Gap
- Polymer Voltage Suppressor Characterization
- Bridging Standards Gap with TLP: GaAs RF Switch
- TLP for OEM Cable ESD
- Summary/Future

Motivation and Purpose

- ESD Characterization of POLYMER VOLTAGE SUPPRESSORS (PVS)
- A TLP method for specifying PVS products to improve Electronic Products:
 - Reliability
 - Mean time before failure
 - ESD Compliance

Motivation and Purpose

- Use of TLP to Bridge the Gap Between Chip and System level ESD Standards
- Increase the use of TLP for ESD equivalent test for:
 - System level ESD Failure Voltage
 - Cable ESD Failure Voltage
 - ESD Compliance using PVS components

System Level ESD Constraints

- Driven by:
 - Smaller semiconductors
 - High frequencies
 - Escalating numbers of signal lines
- ESD is a performance bottleneck
 - Limited chip area and board space
 - Capacitance loads

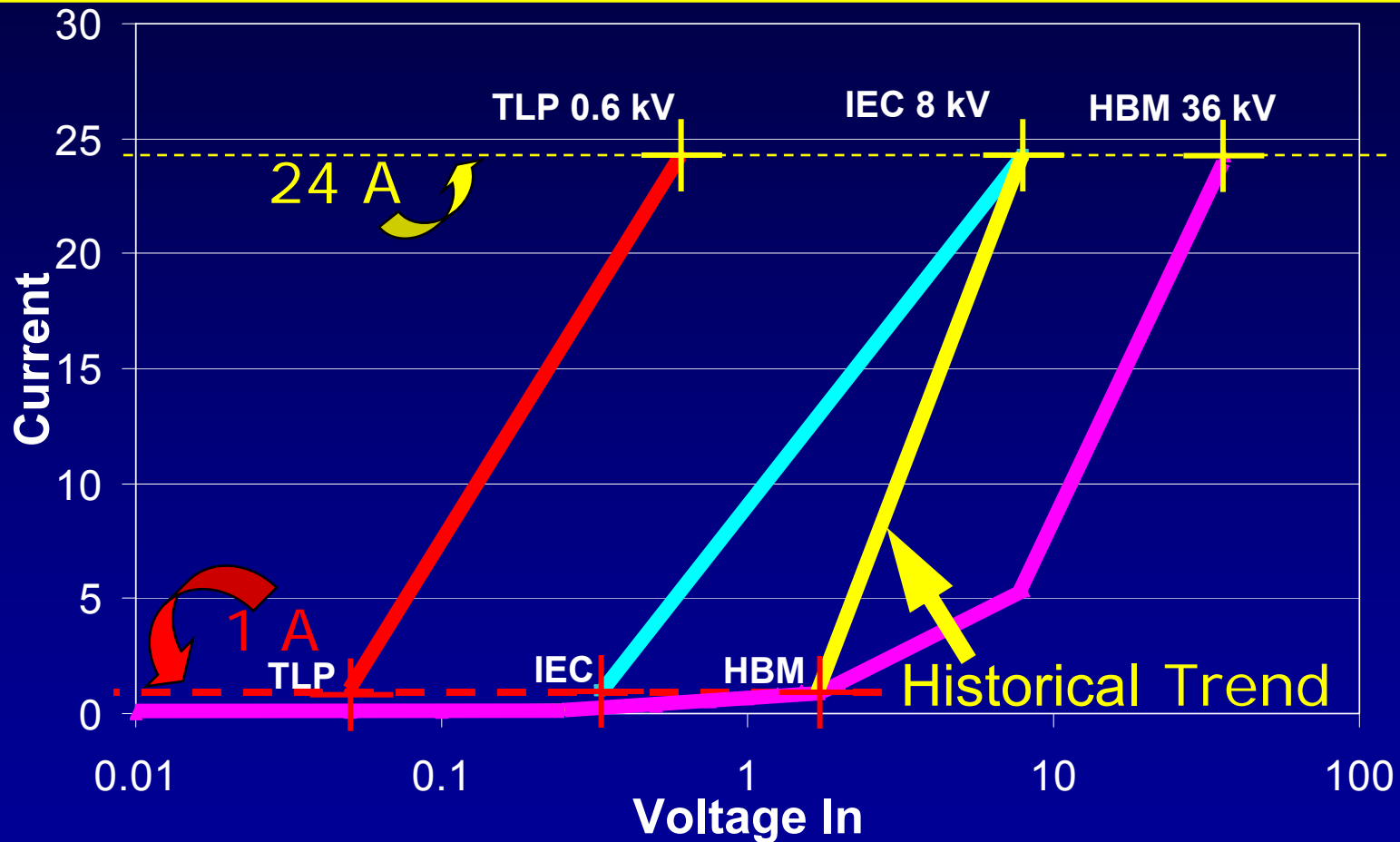
Industry ESD Constraints

- ESD is getting worse
 - On chip protection is failing system level ESD
- RF products need reliability:
 - Cell phones
 - SiGe applications
 - GHz servers
 - GaAs RF switches
 - VCSEL applications
- There is a gap between chip and board level ESD
 - 8 kV IEC has 6X more current than 8 kV HBM

The Standards Gap: On Chip Versus IEC

- Historically Chips were tested at 2000 V
 - 2000 V HBM = 1.3 Amp
 - 1.3 Amp is equivalent to 439 V IEC
- Now: 8 kV IEC is equivalent to 36 kV HBM
- 8 kV IEC = 24 Amp versus 5.3 Amp HBM
- That is the problem
- TLP bridges the gap

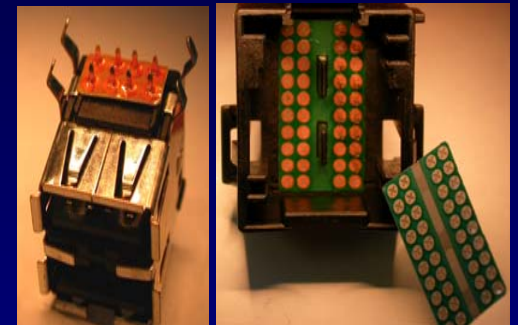
The Standards Gap: On Chip Versus IEC



TLP Bridges the Gap: TLP Correlates to Both

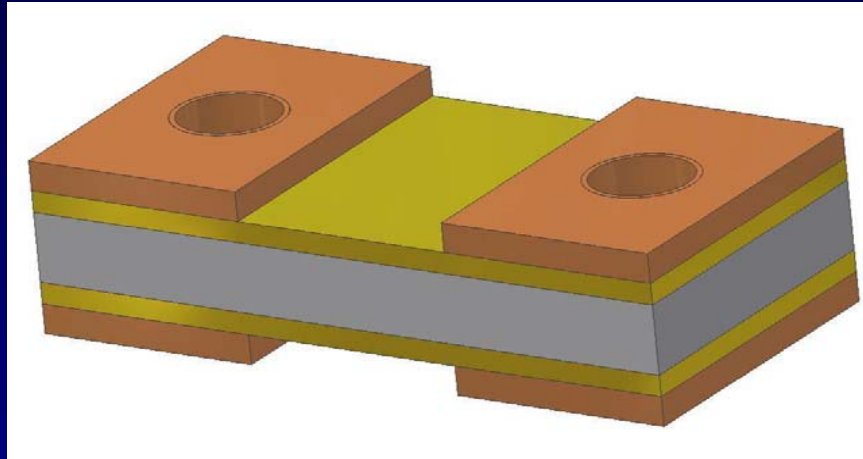
PVS Fits RF ESD Constraints

- Capacitance < 150 fF
- Multiple line ESD protection
- Bipolar
- Low profile, ≤ 10 mils (0.25 mm)
- Pico-second ESD response
- Zero board space on a connector
- Substrateless Surface Mount



**EPI-FLO™ PVS
USB and
Automotive
Connector
Arrays**

Polymer Voltage Suppression Devices



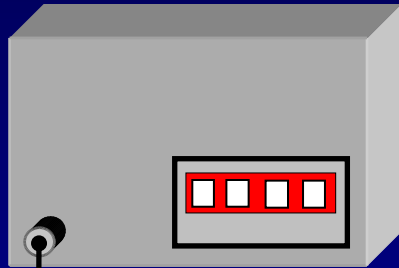
Substrateless Surface
Mount Device

0603 ID#	C _p (fF)
T484A/2/7	102
T484A/2/9	107
T484A/2/45	70
T484A/2/99	118
T484A/2/98	119
T484A/2/95	115
Average	105

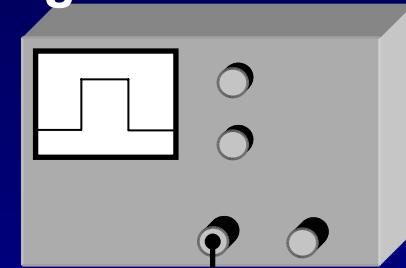
**EPI-FLO™ PVS 0603 Surface
Mount Device Capacitance**

TLP Component Testing

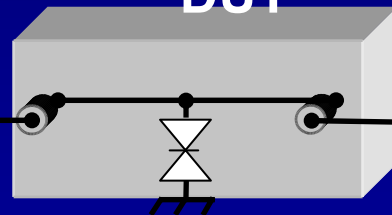
ESD Signal Generator



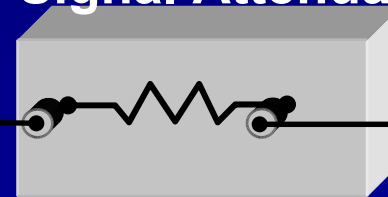
8 GSa / Second
Digital Oscilloscope



DUT

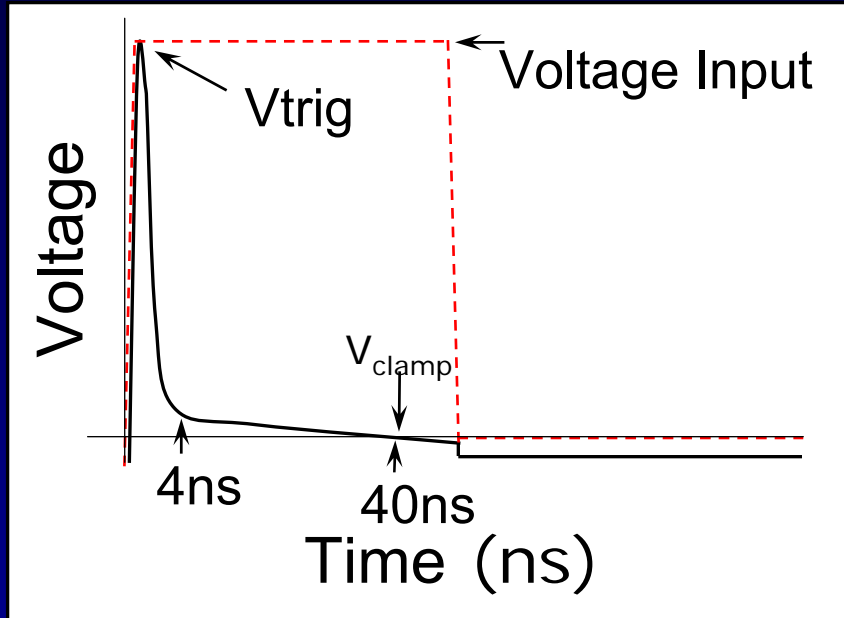


Signal Attenuator



TLP set-up for PVS
and RF components

Surface Mount Voltage Characterization



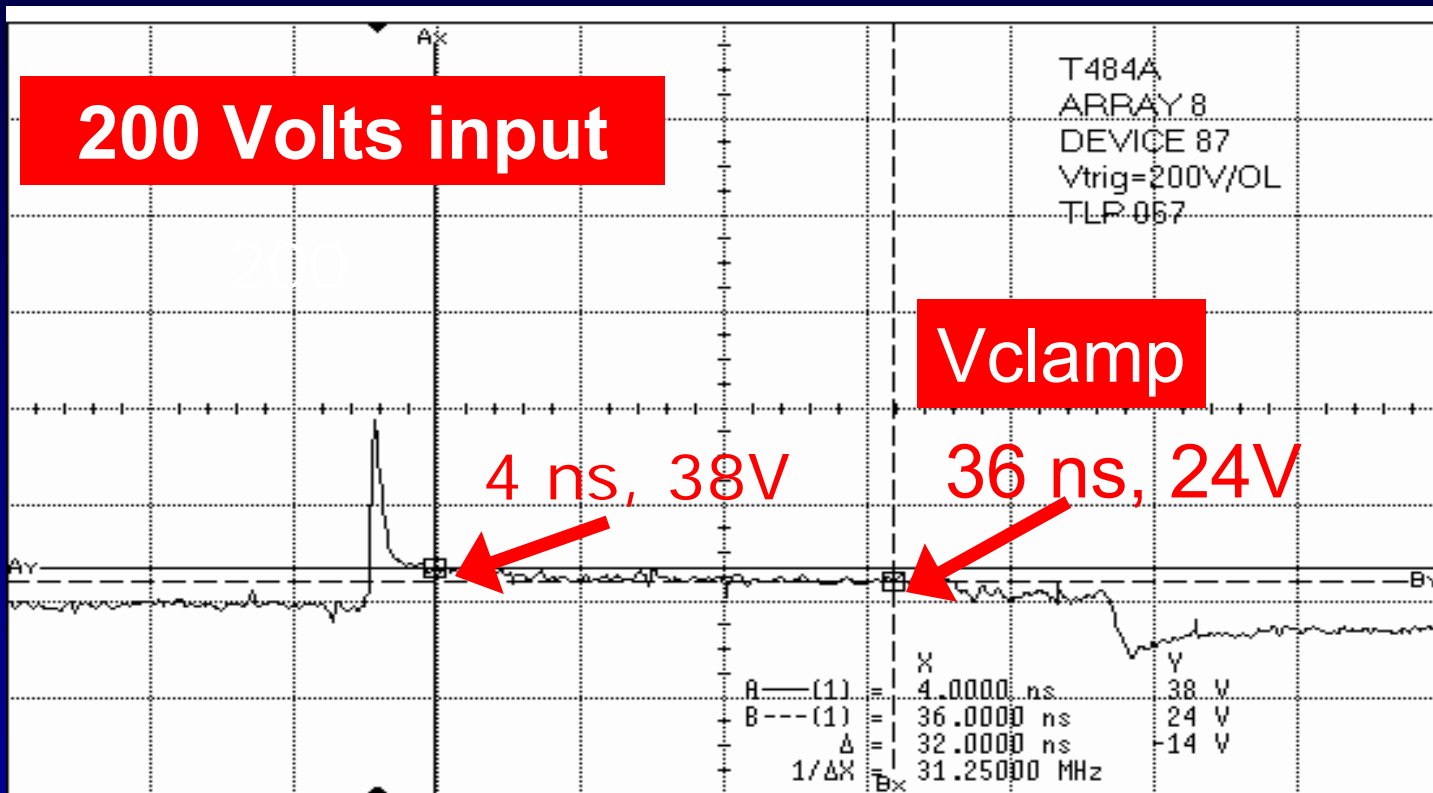
Device	Endurance Test	Vtrig Response	
Vtrig	Endurance, 600V 20th pulse, Vclamp	Vclamp at Trigger	
Volts	$V_{(40ns)}$	$V_{(4ns)}$	$V_{(40ns)}$
100	43	99	30
200	40	181	51
400	48	129	31

100, 200, 400 Vtrig Devices

- Vtrig: Voltage is increased until device turns on
- Endurance: 20x at 600V ~ equivalent to 8kV IEC

TLP PVS Trigger Characterization

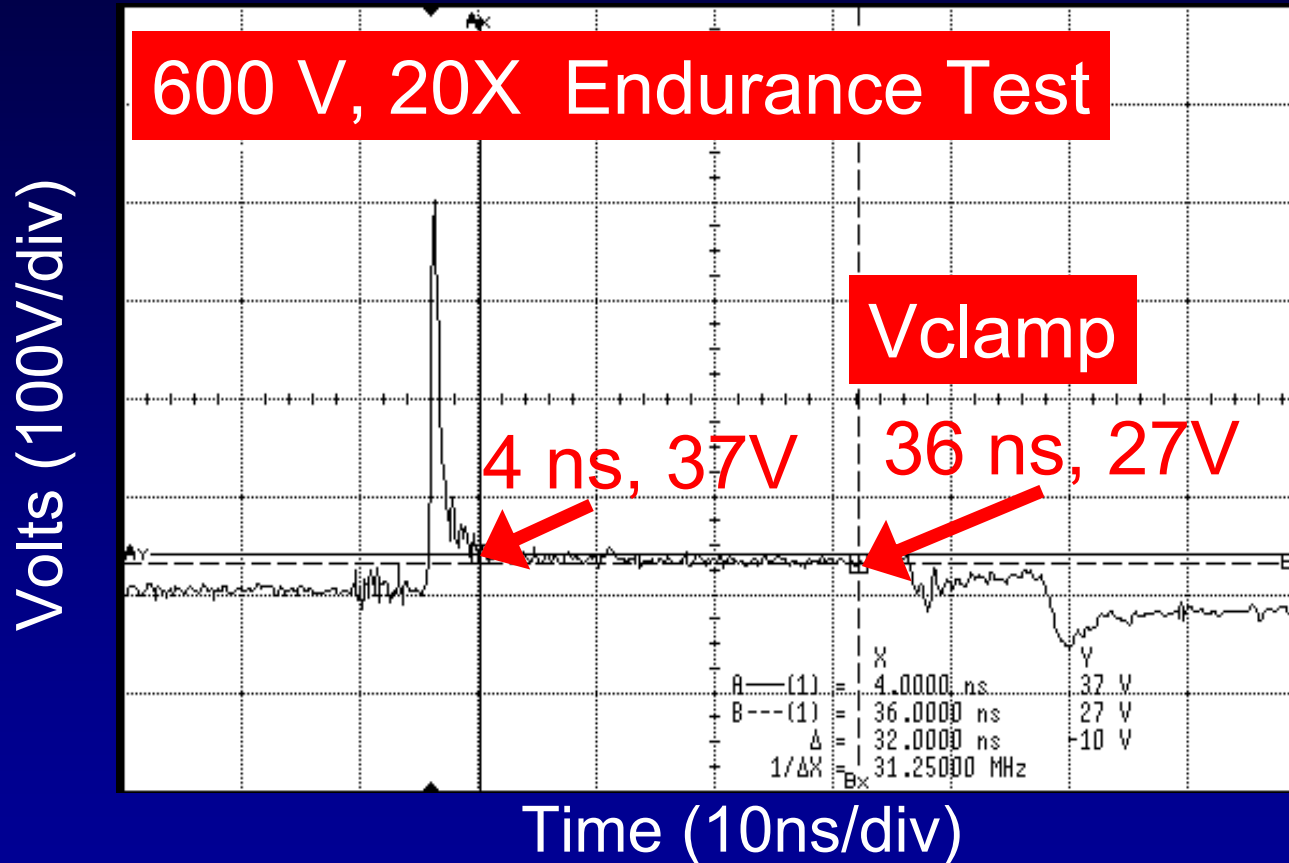
Volts (100V/div)



Time (10ns/div)

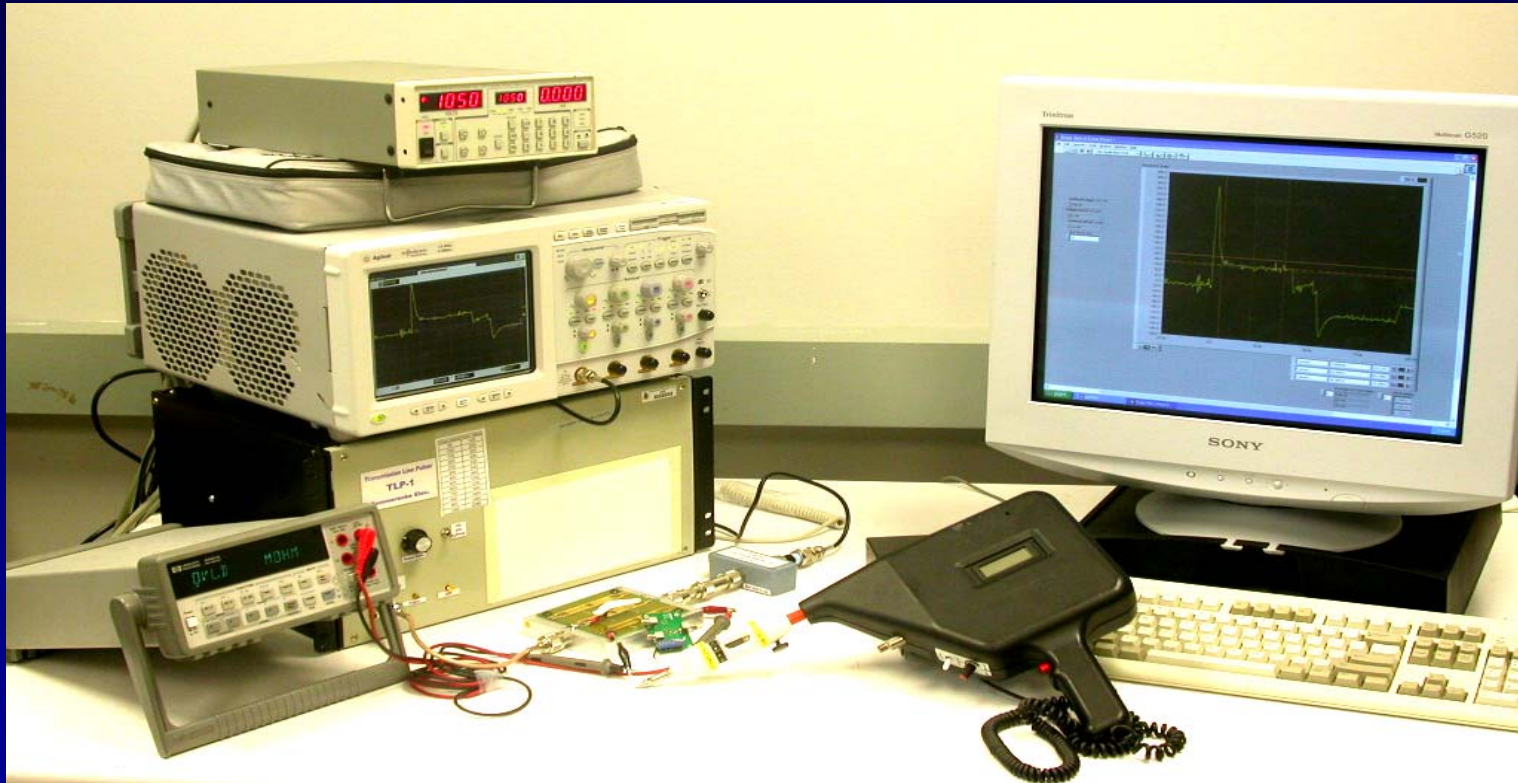
200 Vtrigger 0603 Device

600 V TLP PVS Characterization



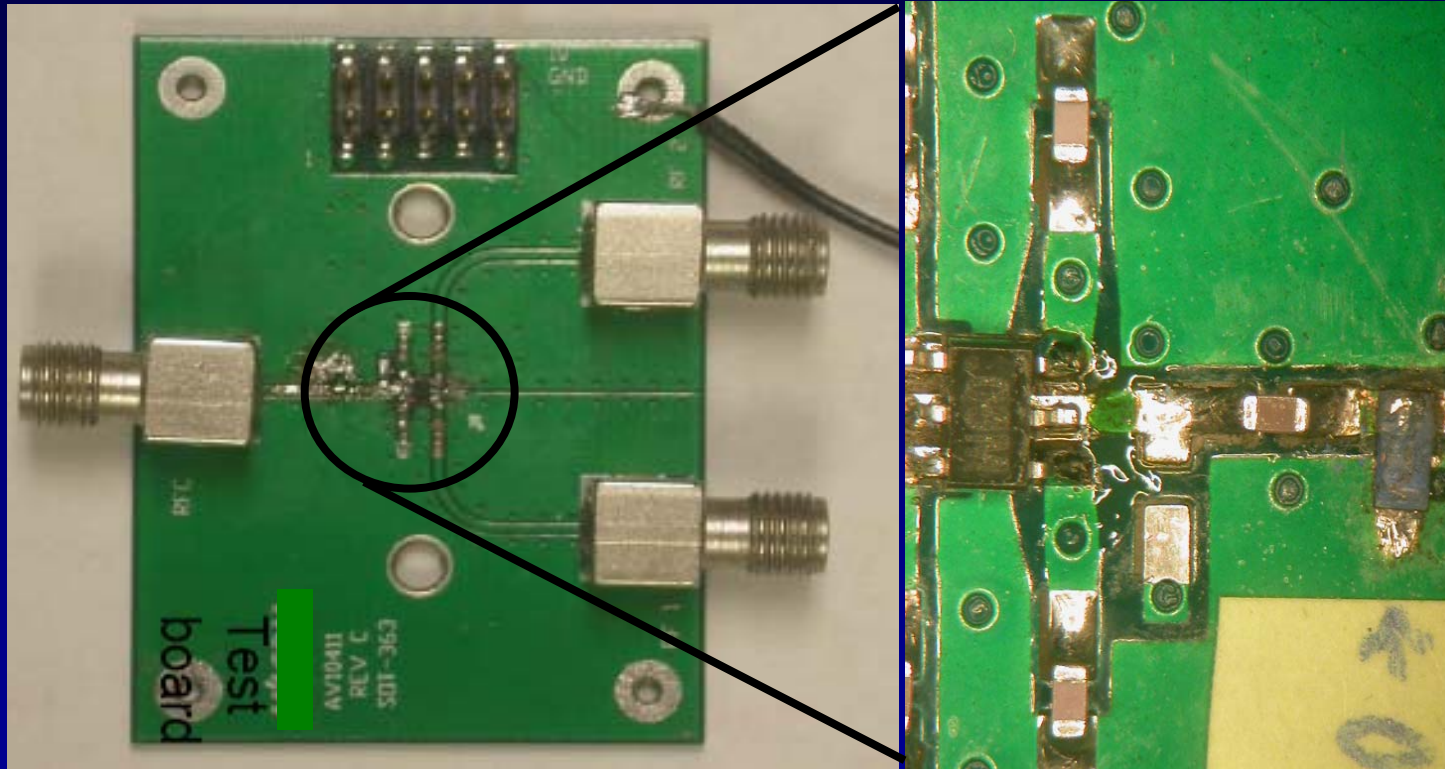
TLP .6 kV Equivalence to 8 kV IEC 6-10004-2`

TLP/ESD System Testing



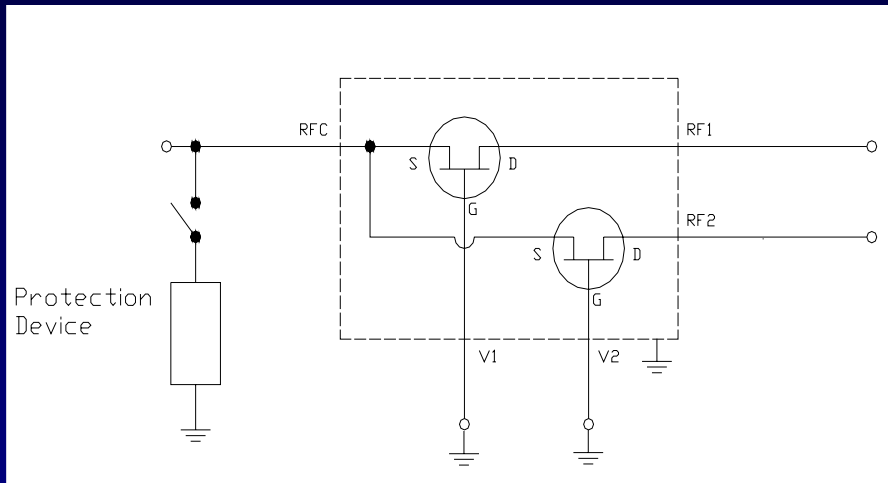
ESD Gun is Added to TLP Testing for Correlation

Cell Phone Antennae Test Board



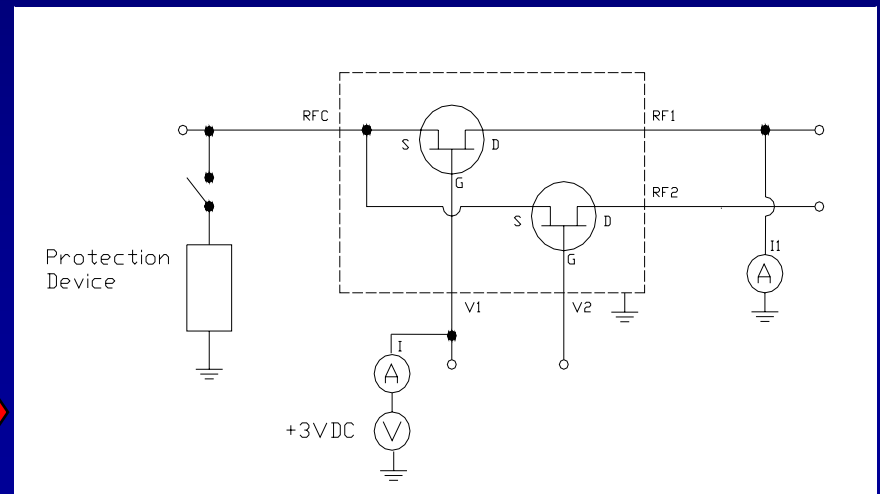
GaAS RF Switch Tested With and Without PVS

TLP/ESD Test for GaAs RF Switch



TLP/ESD gun Voltage
Input on signal line with
and without PVS device
protection

IV Trace: Post ESD/TLP
damage to switch is change
in leakage current when
device is powered.



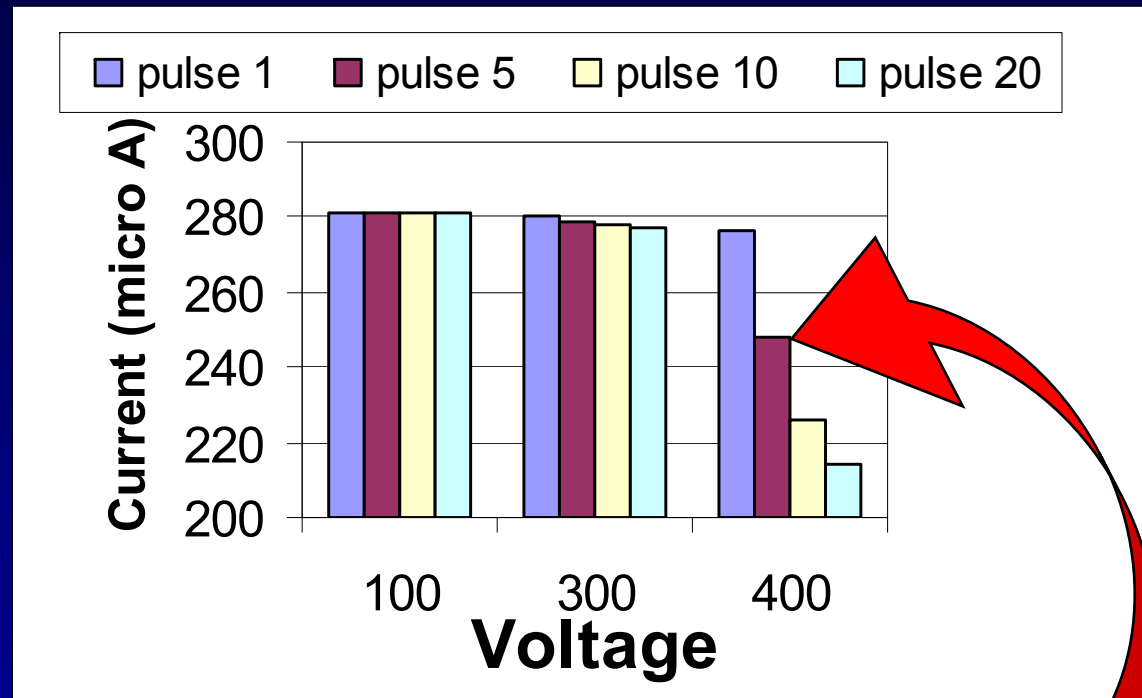
Step 1: GaAs RF Switch ESD Gun

- Zap Gun: IEC 6-10004-2
- Power device
- 10% Change in current at RFC = damaged device

Vin	Pulse #	I (μA)	I (RFC) (μA)	I (RFC1) (μA)	I (RFC2) (μA)	Open Circuit I (μA)
100V	1x	281	281	281	281	0
	5x	281	281	281	281	0
	10x	281	281	281	281	0
	20x	281	281	281	281	0
300V	1x	280	280	280	280	0
	5x	279	279	279	279	0
	10x	278	278	278	278	0
	20x	277	277	277	277	0
400v	1x	276	276	276	276	2
	2x	276	276	276	276	4
	5x	277	248	248	248	253
	10x	277	226	226	226	265
	20x	277	214	214	214	268

Step 1: ESD Gun Test GaAs RF Switch

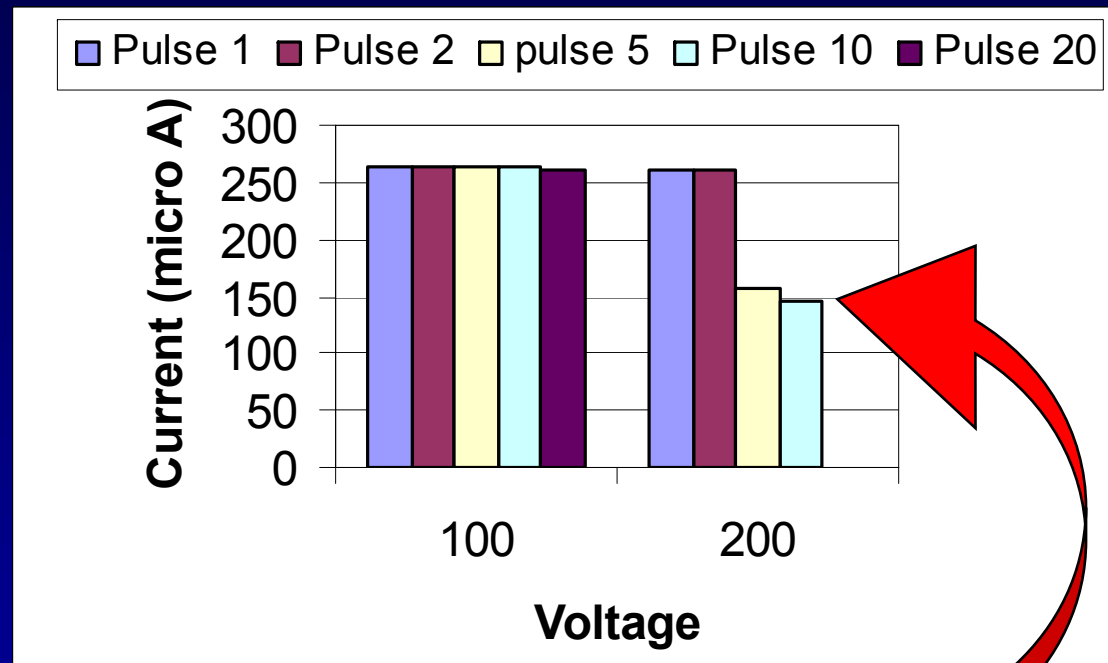
- Pulse
 - 1X, 5X, 10X, 20X
 - Ramp V by 100V
- Failure = 10% change in RFC current



Failed Current < 253 μ A

Step 2: TLP Test GaAs RF Switch

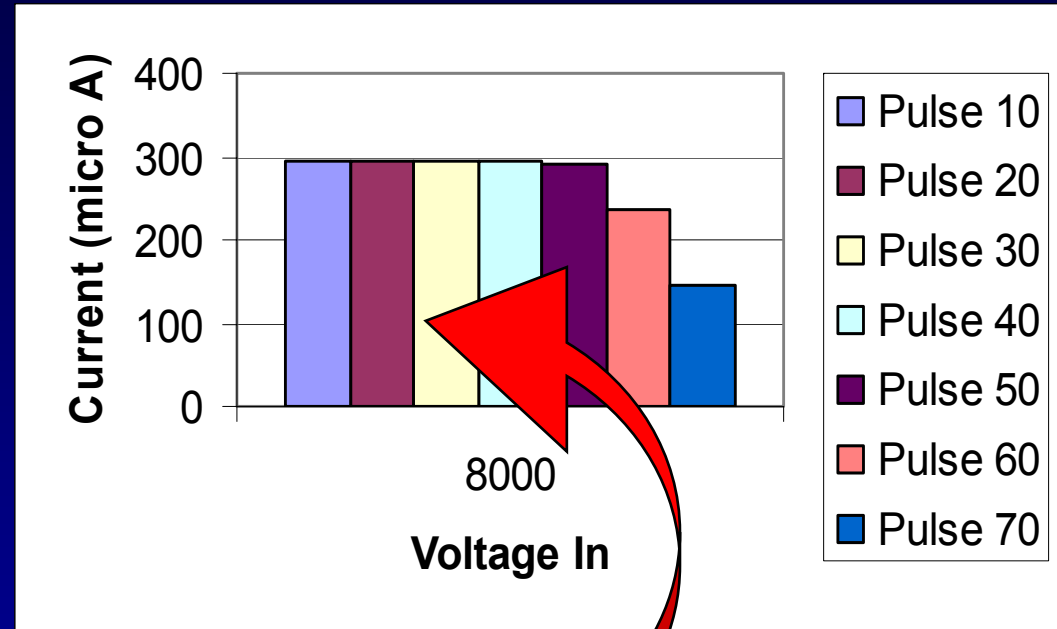
- Pulse
 - 1X, 5X,
10X, 20X
 - Ramp V
by 100V
- Failure = 10%
change in
RFC current



Failed Current = 158 μ A

Final Step: 8 kV IEC Test with PVS

- Select PVS device
Vtrig < 200V
- Solder PVS device
on board
- Zap 20X+ at 8 kV
for ESD compliance

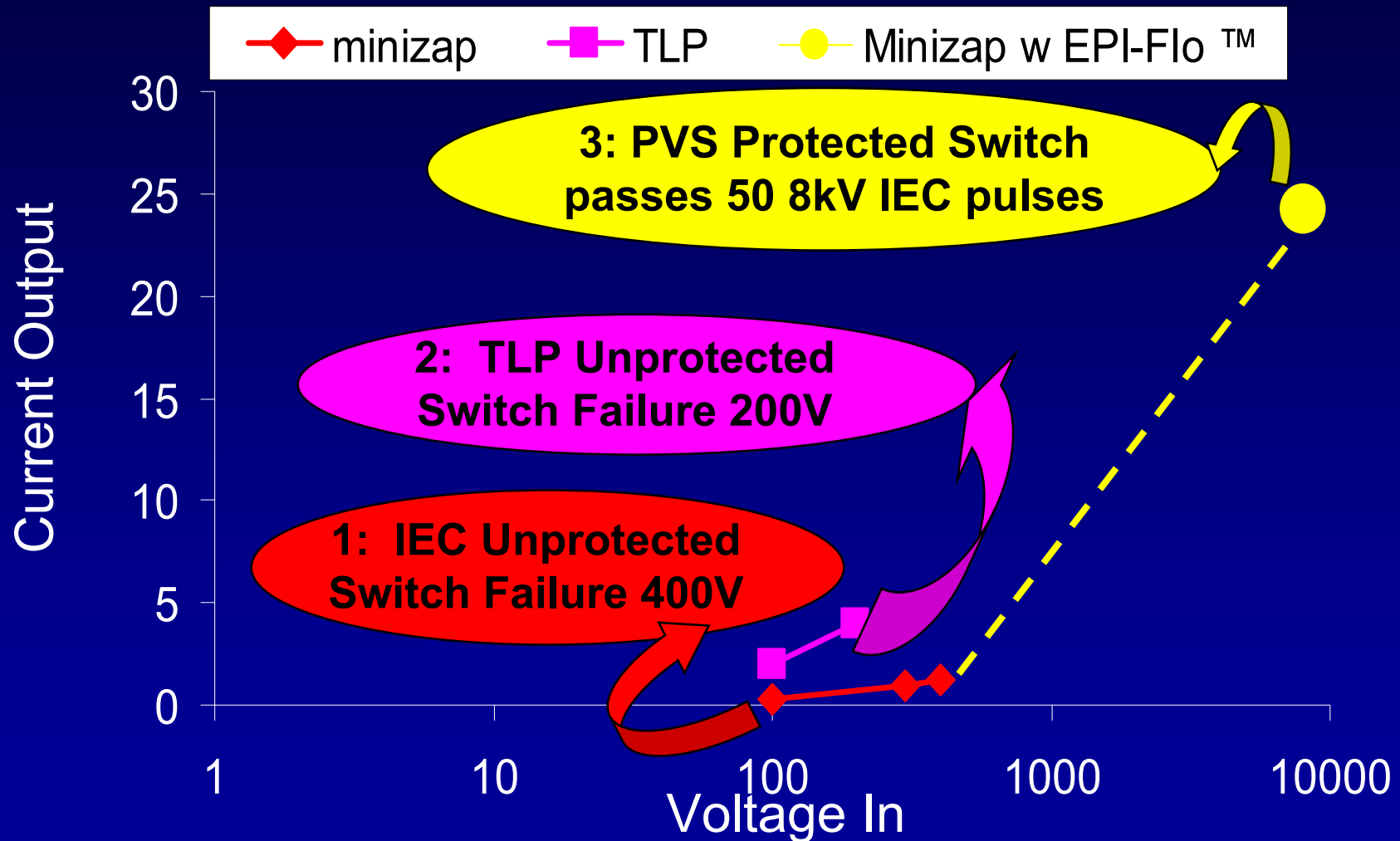


20 Pulses = IEC Requirement

Failure = 158 µA

GaAs Switch With 100Vtrig PVS Undamaged

TLP Test Method Summary



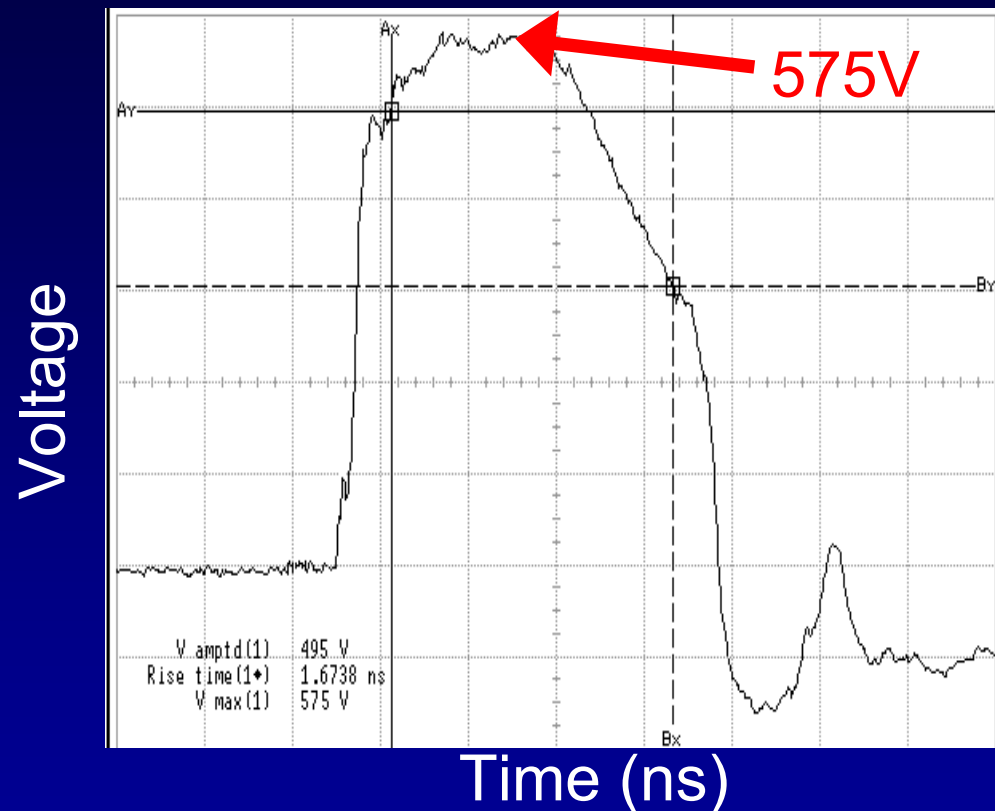
VCSEL HBM/TLP Test Result

VCSEL # Avg. 5 devices									
Initial Voltage		Current In		Current Out		V4ns		V40ns	
3	V DC only	12.19	mA	332.40	μ A	N/A	V	N/A	V
10	V pulse	12.00	mA	324.00	μ A	9.33	V	9.69	V
15	V pulse	12.00	mA	324.00	μ A	13.27	V	15.02	V
20	V pulse	12.06	mA	326.00	μ A	15.52	V	18.76	V
25	V pulse	12.05	mA	326.80	μ A	18.56	V	21.46	V
30	V pulse	12.06	mA	326.00	μ A	21.01	V	24.20	V
35	V pulse	12.03	mA	325.00	μ A	23.12	V	26.19	V
40	V pulse	12.02	mA	324.20	μ A	25.06	V	27.39	V
45	V pulse	12.00	mA	324.00	μ A	27.36	V	29.76	V
50	V pulse	12.01	mA	322.60	μ A	29.17	V	32.46	V
55	V pulse	11.99	mA	304.40	μ A	31.85	V	34.52	V
60	V pulse	12.02	mA	254.60	μ A	33.69	V	36.49	V
65	V pulse	12.01	mA	149.20	μ A	35.56	V	37.88	V
70	V pulse	12.02	mA	74.40	μ A	37.50	V	39.23	V
75	V pulse	12.05	mA	34.65	μ A	39.37	V	41.29	V

**Photo Diode Current Output Showed PVS
with Vtrig <60 V Required for 1000 V HBM**

Cable ESD Tests Need Standards

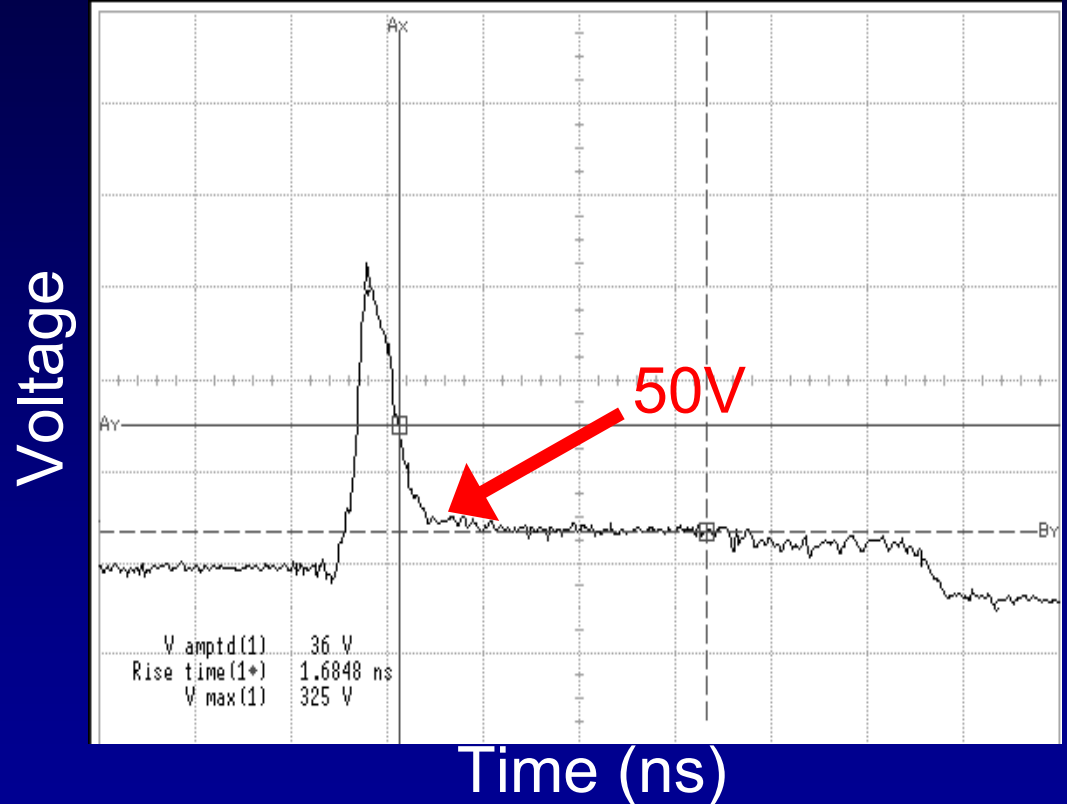
- Cable ESD varies:
 - Automotive:
 - 25 kV IEC
 - 10 kV TLP
 - Giga bit server:
 - 600 foot cable charged to 3kV



600V TLP test of RJ-45 connector with Magnetics shows no protection

Cable ESD PVS Specs \neq IEC ESD

For Cable ESD for Server application PVS Device on RJ-45 connector needs to be tested with 600 foot cable charged to 3 kV



PVS installed on RJ-45 removes ~80% of 8 kV equivalent ESD TLP pulse

The Future

- Low Capacitance PVS devices remove performance barriers for :
 - Cell phones, Giga bit servers, PDA's
 - SiGe, GaAs, InP, semiconductors
 - Tunneling Magneto Resistive Heads
- PVS devices open doors for future sensitive semiconductors removing ESD as a potential barrier to Market entry

Summary

- The gap between chip and system level ESD standards needs a TLP standard
- TLP/ESD characterization using femto Farad Polymer Voltage Suppression devices provides 8 kV IEC reliability for of RF products and components
- PVS devices open the door for future sensitive semiconductors removing ESD as a potential barriers to Market entry