Transmission Line Pulse Test Methods, Test Techniques and Characterization of Low Capacitance Voltage Suppression Device for System Level Electrostatic Discharge Compliance

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Abstract – Voltage suppression devices are needed in electronic systems to prevent damage to electrical components from electrical overstress (EOS) and electrostatic discharge (ESD) events. A low capacitance, polymer voltage-suppressor (PVS) device is evaluated using various testing techniques that combine transmission line pulse (TLP) test system, direct discharge HBM, and a system-level ESD gun. Additionally, test methods for integrating PVS devices for system-level ESD protection of cell phone GaAs radio frequency (RF) switches and Gigabit Ethernet server semiconductors will be shown. Our work demonstrates the need for integration of device-level and system-level test methodologies for correlation between component ESD survivability and system-level ESD concerns.

I. Introduction

With the trend towards smaller semiconductor chip geometries, higher functional frequencies, and the escalating number of signal lines, system-level ESD issues on products have increased. At the same time, both the allocated space and the capacitance budgets that circuit designers allow for on-chip ESD protection devices are decreasing [1]. The capacitance of an ESD protection component is a critical characteristic because too much capacitance degrades high speed digital signals and influences the frequency response of RF components. The capacitance requirements for RF receivers on GHz signals are hundreds of femto-farads (fF) and these requirements decrease with each technology generation. The more stringent capacitance requirements creates a potential performance-ESD conflict for use of traditional protection components and may lead to an ESD roadblock in future technology generations for digital and RF technologies. With increasing number of I/O circuits, the amount of real estate needed for ESD protection on semiconductor input/outputs (I/Os) and on PCB I/Os increases, making the ESD protection strategy challenging and a potential bottleneck [1].

System-level ESD protection for all signal lines in both hand-held and fixed electronics is emerging as a major requirement for improving product reliability and mean-time-before-failure (MTBF); both can impact a company's profitability through customer dis-satisfaction and product field returns. Hand-held devices such as PDA's, cell phones, and fixed electronic systems such as computers and servers are constantly exposed to system-level ESD during handling and information-transfer processes (e.g., docking a PDA). Electronic boxes, for example, fast Ethernet servers can have hundreds of lines that need protection from ESD cable discharge events (CDE). CDE occur when plugging in charged cables into high performance GHz servers leading to ESD and latchup issues [2, 3]. In GHz server applications, reliability is a key issue, and ESD CDE can be even more damaging than system level IEC 61000-4-2 ESD events. Even in the automotive industry use of semiconductor electronics has exploded to include engine control modules, security systems, windshield wipers, and GPS devices; all of these functions require high ESD reliability in the face of high current or high energy ESD-like pulses. Additionally, equipment-end users do not want to re-boot cell phones or computers, or worse yet, lose data and time as a result of component damage caused by system-level ESD events [4].

To enable ESD protection of electronic products, PVS devices were designed with low capacitance and space efficient packages for multiple-line ESD protection. PVS devices incorporate system-level ESD protection without interfering with GHz signals, or taking a lot of real-estate on a printed circuit board (PCB) or on-chip die. The connector manufacturer roadmap includes taking components off the PCB and installing them where possible on the connector to optimize utilization of PCB area. PVS arrays assist in reducing the number of ESD protection components on the board by incorporating the array in or on the connector.

Integration of PVS devices into components and products for system-level ESD protection has required the development of TLP test equipment and ESD procedures for correlation of PVS device over-voltage performance to HBM and IEC 61000-4-2 ESD standards [5, 6]. System-level ESD tests (as defined by IEC 61000-4-2) has a source impedance (SI) of 330 Ω; therefore at 8 kV, a current of 24.24 A is discharged directly. In comparison, an 8 kV HBM event has a SI of 1500 Ω; at 8 kV the current is 5.3 A (approximately 4.5 X lower current). Many semiconductor chip manufacturers design to a 2 kV HBM ESDA specification, and as high as a 8 kV HBM protection level for controlled environment semiconductor chip packaging and assembly, but due to a high peak current of system level ESD, 8 kV HBM does not protect from 8 kV system-level ESD or CDE encountered during equipment handling. CDE varies by product, and is usually more energetic than either HBM or IEC 61000-4-2, exhibiting either a higher current level, faster rise time, or longer pulse duration. For example, an automotive specification may use a 25 kV direct discharge IEC 61000-4-2 ESD event.

As a result of the higher currents present in system level ESD, the on-chip protection system for HBM ESD usually fails system-level ESD pulses unless there is an ESD PCB protection component. To use PVS devices for system-level ESD conformance we developed test procedures and equipment to measure the ESD gun and TLP input voltage that causes a sensitive component to fail (when powered post-ESD pulse test). In our work, we first correlate PVS device TLP pulse endurance (20 pulses) to system-level ESD. Next, we select a PVS with a lower TLP turn-on voltage (Vtrigger) than the TLP voltage that caused the device under test (DUT) to be damaged. Using this protocol, we have installed a PVS device and brought components that fail the system ESD test into compliance.

A unique ESD test procedure we developed combines traditional testing practices used for design of HBM ESD on-chip ESD protection [7] with a TLP test method that correlates to the pulse delivered by a system-level ESD gun pulse. This paper first discusses the PVS technology and the attributes that make it suitable for ESD protection of today's systems and components. Second, the paper describes the TLP equipment and test procedures used to characterize PVS ESD performance and Vtrigger condition. Third, the test procedures and equipment used to increase a GaAs RF switch survivability from 5 pulses at 400 V to over 50 pulses at 8 kV by incorporating a PVS device with a 100 V Vtrigger are presented. The test methods for implementing the PVS protection demonstrate a method of correlating TLP susceptibility of semiconductors to the survivability needed for system level ESD compliance. Using an equivalent procedure, similar experimental results are shown for a 3 GHz GaAs Vertical Cavity Surface Emitting Laser (VCSEL) and for a PVS device mounted on a RJ-45 connector to protect PCB signal traces leading to a sensitive IC on a Gigabit Ethernet server PCB.

II. Polymer Voltage Suppression Electronic Device

The need for economical ESD protection of multiple signal lines along with the need for low capacitance at high frequencies fits the characteristics of PVS components. Traditionally, devices used for ESD include low capacitance air gaps, resistors, capacitors, inductors, varistors, double-diode ESD elements and combinations thereof. Diodes were commonly used until the need for low capacitance and high current ESD protection emerged. As the ESD pulse increases, the ESD diode size is usually increased. System-level diode capacitance is usually 5 pF unless multiple diodes are used; multiple diodes increase cost and device size [8]. Although diodes are capable of extremely low trigger voltages, the capacitance can cause signal distortion, and the space required to protect 100's of IO's on a PCB or on the semiconductor chip is expensive.

In PVS components, the low dielectric constant of the polymer provides inherently low fF capacitance. The dielectric constant of the polymer film can be formulated to meet application requirements ranging from MHz to high GHz frequency ranges. In this paper, the PVS devices tested are either EPIFLO™ surface mount devices with an 0603, or 0402 footprint, or EPIFLO arrays for insertion on

connector signal pins (RJ, USB, MQS, backplane) [9].

Figure 1 shows the construction of a single unit PVS surface-mount device consisting of a PVS film laminated between electrodes. Since PVS devices are bipolar, a single device soldered on a PCB or component signal line shunts positive and negative voltage surges from signal line through the PVS to ground.

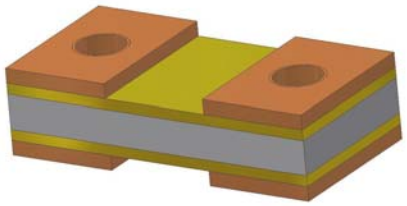

Figure 1: PVS Construction for 0603, 0402, 0201 Surface Mount Device

The PVS film used consists of an epoxy polymer, containing uniformly-dispersed conductive and non-conductive particles, laminated between electrodes. The laminate is transformed into a device using a process similar to that used for manufacturing PCBs. The PVS device's overall thickness is in the less than 10 mil range. The PVS material does not require a substrate and, consequently, the trigger voltage of the device is set by device dimensions and the polymer formula.

PVS component package style includes single- and multiple-array surface mount components, and connector arrays. Low profile, multiple device connector arrays are inserted on connector pins by press fit or soldering. Installing the protection array on the connector provides ESD protection right at the input of the PCB (at the input traces of ESD sensitive components and semiconductors). Arrays are designed to be on the side of the connector that is exposed to the outside world.

Each array is customized to fit on specific connectors. Universal Serial Bus (USB) connectors have four signal line pins to which EPIFLO arrays are mounted to provide ESD circuit protection. An RJ-45 array for a Gigabit 1000 BASE T Ethernet server can have an 8X array (equivalent of 8 lines protected) mounted on 8 signal pins for a single RJ or as large as a 64X array for 64 signal lines on connector consisting of 8 RJ ganged together. In Figure 2 the MQS engine control automotive connector has a 40X array with one of the 40 pins serving as the ground pin. The connector contains installation alignment pins.

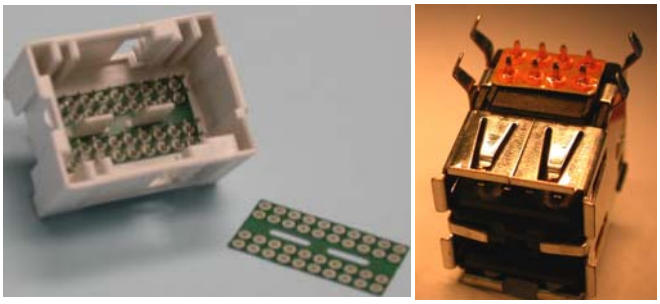

Figure 2: ESD Connector Array on 40 pin MQS automotive engine control module connector and 8 pin USB connector.

Table 1 indicates the capacitance of a PVS 0603 Surface Mount is approximately 105 fF. Since low capacitance is a requirement for GHz applications, we have tested PVS device protection for a GaAs RF switch (for use in cell phones), and a 3 GHz GaAs VCSEL (used for conversion between optical and electronic data in high speed fiber optic networks). Typical capacitance for PVS 0603 surface mount components used is less than 150 fF.

Table 1: 0603 PVS Surface mount capacitance.

Device ID	Vtrig	Cp (fF)
T484A/2/7	200	102
T484A/2/9	200	107
T484A/2/45	200	70
T484A/2/99	200	118
T484A/2/98	200	119
T484A/2/95	200	115
Average	**200**	**105**

Through process formulation and package geometry changes, capacitances as low as 10 fF have been achieved. Capacitance on a connector array is typically 1 pF due to a larger ground plane.

The PVS device response time is extremely fast. Measurements taken using an 8 GSa/s scope show that PVS devices respond in less than 200 pico-seconds and the time to clamp is less than 10 ns. Figure 3 shows the majority of a 600 V TLP pulse is clamped in less than 4 ns to 37 V. At 36 ns, the pulse is clamped to 27 V. The 600 V TLP pulse is equivalent to an 8 kV ESD system level pulse. The PVS material needs to be extremely fast to provide protection to ESD standard pulses that rise to thousands of volts in nanoseconds or sub-nanosecond time scales.

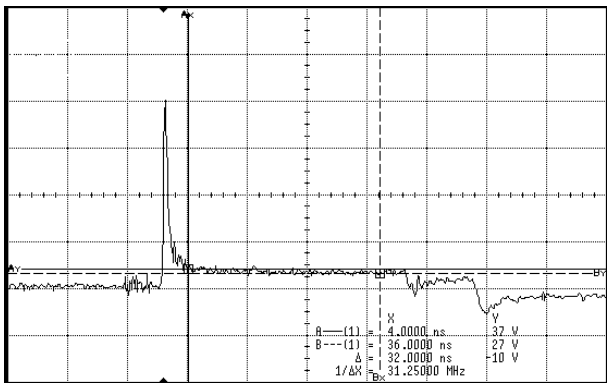

Figure 3: 0603 PVS device clamps 600 V TLP to 27 V

PVS devices are ESD robust and capable of withstanding hundreds of ESD pulse events. The volume of material needed to withstand an 8 kV ESD pulse was determined by calculating the volume of material used in an 0302 surface mount device to provide 8 kV protection and found to be ~140 cubic mils (1.40E-06 in^3). PVS devices with large ground planes and 400 Vtrigger, have protected automotive components from a 25 kV ESD gun direct discharge per IEC 61000-4-2.

Figure 4 shows a 200 $V_{trigger}$ 0603 PVS device performance with 200 V_{input}. A 200 Vtrigger means the device does not trigger until 200 V, but at 200 Vtrigger the TLP pulse was clamped to 38 V in 4 ns; and to 24 V at 36 ns. This device is the same device tested in Figure 3 which was tested at 600 V TLP, where V_{clamp} is 37 V, and 27 V in 4 and 36 ns, respectively. The test system used for measuring the device characteristics is critical to obtaining the reproducible clamp voltages at different TLP pulse voltages.

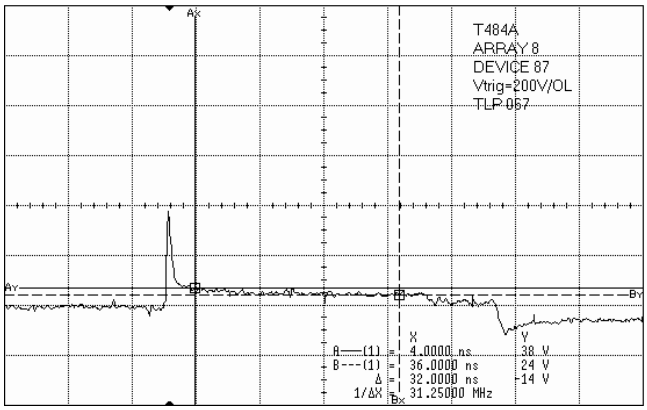

Figure 4: 200 Vtrigger 0603 PVS response to 200 V TLP.

III. TLP and ESD Gun Equipment Set-Up and System Level ESD Test Procedure

A. Test Set-Up

Test measurements are performed using equipment configured as shown in Figure 5, consisting of a TLP, a fixture (50 Ω impedance) for connecting to the DUT, a special high-voltage signal attenuator and an oscilloscope with high-bandwidth single-event performance. This is a controlled impedance environment at 50 Ω using coaxial cable for interconnect. The TLP system is capable of generating rectangular voltage pulses up to 2000 V at a Thevenin equivalent source impedance of 25 Ω (4000 V pulse from a 50 Ω source terminated in 50 Ω) at a pulse width (48 ns in this case) determined by the length of a time delay coaxial cable. The oscilloscope has sufficient bandwidth and sample rate to accurately display transient rise times down to 200 ps. The signal attenuator is required to drop the signal level to the oscilloscope's dynamic voltage range.

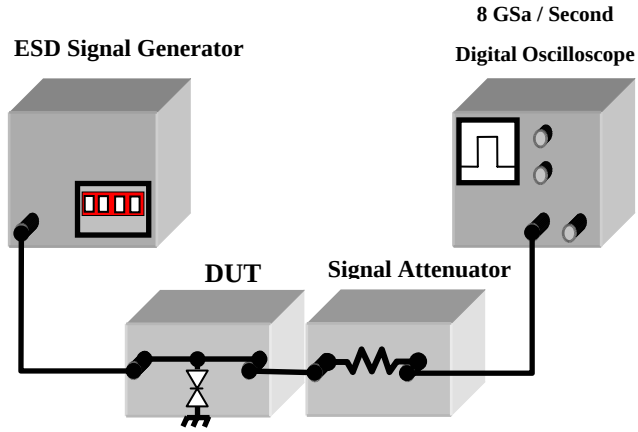

Figure 5: TLP set-up

When testing with a mini-zap ESD gun and ESD system-level pulses, it is much more difficult to view the waveforms on an oscilloscope because of the high E and H fields generated by the gun; additionally, its cabling causing a false representation on the oscilloscope of the real event. The configuration would generally require a high impedance probe (relative to the 330 Ω output impedance of the gun) and Faraday shielding of either the gun and DUT or the probe and oscilloscope. Because of this difficulty, the test method used was to disconnect the DUT fixture from the TLP set-up and perform the ESD gun test without viewing the results. After pulsing, the

DUT was tested for failure in the same manner as with the TLP set-up.

Table 2 shows how we use current to establish the TLP voltage needed to simulate either the IEC 61000-4-2 ESD pulse or a HBM pulse. The main difference between the TLP and the two ESD gun pulses used is the source impedance (SI) and the pulse waveform. HBM discharges 150 pF through a 1500 Ω SI, while IEC 61000-4-2 discharges 150 pF through 330 Ω. The ESD gun pulse shape is a double exponential with capacitive time constant T_C = RC. The HBM pulse is 4.5 X longer than the IEC 61000-4-2 system level pulse. In our TLP test set up, we use a cable length of 48 ns to simulate the pulse duration of system level ESD event. As an example, to simulate the 24 A output by 8 kV IEC 61000-4-2 the TLP is set at 600V.

Table 2: Input TLP Voltages for simulation of IEC and HBM

Transmission Line			Industry Specification Methods			
SI (Ω)	V (V)	I (A)	Industry Specification	SI	V (kV)	I (A)
25	150	3	HBM 4kV	1500	4	2.7
25	250	5	HBM 8kV	1500	8	5.3
25	300	12	IEC 61000-4-2	330	4	12
25	600	24	IEC 61000-4-2	330	8	24
25	1900	76	IEC 61000-4-2	330	25	76

During TLP testing of a DUT, the voltage trace is recorded to observe the change in DUT clamping response as the TLP pulse voltage is increased. Often an increase in the clamp voltage is observed during a pulse when a device is reaching its damage threshold. It will appear that the device current handling capacity has been saturated. Post-pulsing evaluation of the powered DUT confirms the damage much more clearly than the TLP traces of successive pulses.

Figure 6 shows the bench-top test setup used to characterize a DUT and the PVS used for providing system-level compliance. Actual set up shown was for testing a GaAs RF GHz switch. The setup readily allows change between the TLP and the mini-zap gun.

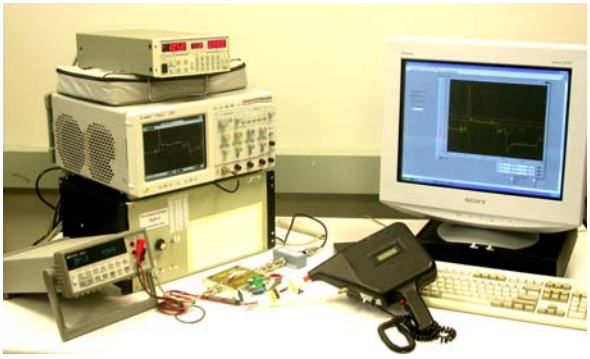

Figure 6: ESD Gun and TLP used for system level tests of components

B. System Compliance Test Procedure

The procedure we use to obtain the specification for a PVS device that provides a component or semiconductor with system-level ESD compliance is similar to the TLP testing we use for PVS device characterization except the component to be protected is tested for damage while powered, and damage criteria are provided by the device manufacturer or the system manufacturer.

A three step test procedure is used to raise ESD sensitivity of a GaAs RF switch for use in a cell phone from 400 V to 8 kV using a PVS component. First, the GaAs RF device is pulsed 20 times with direct discharge ESD Voltage using IEC 61000-4-2 ESD gun; voltage is increased until failure voltage is reached as measured by a 10% increase in RF switch leakage current under power. Second, using the TLP, the GaAs RF device is subjected to increasing voltage pulses to determine the TLP failure trigger voltage and clamp voltage. Damage is determined as with the ESD gun, by a 10% increase in the RF switch leakage current. The TLP damage voltage is usually lower than the ESD gun damage voltage due to correlation between the 2 test methods not being exact. Third, a PVS component with a lower trigger voltage than the GaAs RF TLP failure trigger voltage is added to the circuit for DUT protection. Protection is then verified by ESD gun testing to 8 kV IEC ESD.

IV. Testing of Voltage Suppression Electronic Polymer

We have found that in order to protect a semiconductor chip or other sensitive components such as high frequency GaAs chips, our PVS component must turn on at a lower voltage than the semiconductor chip protection diode, or in the case of a GaAs RF switch in which there is no designed in protection, at a voltage lower than the ESD failure voltage. The PVS device must also turn on within

nano-seconds, preferably in pico-seconds. We have found that if a PVS device is not fully turned-on within nano-seconds, the ESD pulse rise is so rapid that the protection on the semiconductor chip will turn on and the semiconductor will fail once the current exceeds the HBM designed in protection.

These criterion have been responsible for the evolution of our PVS device test methods. During the initial test procedure development using GaAs VCSELS we learned that it was critical to observe clamp voltage as well as trigger voltage. The requirement was for HBM ESD protection at 2000 V. The current procedure for testing PVS components performance has proven capable of defining the PVS Vtrigger needed for system level ESD conformance of sensitive components.

The first test run on the PVS device is a ramped voltage test to establish the voltage trigger at which the device repeatedly shunts the voltage to ground. If the PVS device does not trigger there is no change in the input voltage. The second test is an endurance test to determine the PVS component can withstand over 20 ESD pulses equivalent to 8 kV IEC, and the third is a re-test; this is to assure the trigger voltage has not changed. Life testing has been run during which the device is tested for 100, then 1,000 pulses equivalent to 8 kV direct discharge. In our testing we still find that the TLP test is more severe than the direct discharge ESD pulse from the mini-zap gun. As we clean up the reflections in the TLP test, the correlation between the two test methods improves. Typical clamp voltage data for different Vtrigger PVS devices are shown in Table 3.

Table 3: TLP test method for PVS devices

Device	Endurance, 600V20 x 20X	V-Trigger	
0603	40ns (V)	4ns (V)	40ns (V)
100Vt	43	99	30
200Vt	40	181	51
400Vt	48	129	31

Note that trigger voltage data is taken at 4 ns to assure device speed, and at 40 ns for the device clamp. The data shown is a 100 V trigger device that protects a GaAs RF switch, a 200 V device that does not protect the same type of GaAs RF switch, and a 400 V device for automotive cable ESD of 25 kV air discharge.

V. Testing of GaAs RF Devices

To determine how to protect a GaAs RF switch for use in a cell phone, the following test procedure was used. The GaAs RF switch was tested with a Keytech Mini-zap Model MZ-15/EC designed for IEC 61000-4-2. Testing was started at 100 V input and continued through 400 V using 100 V increments. The device was tested for 20 pulses at each voltage, and tested for leakage current under power after 1, 2, 5, 10, and 20 pulses. A 10% change in RFC current or in open circuit leakage current was considered a failed device. The device began to show damage on the first 400 V pulse, and was completely damaged between 3 and 5 pulses. In Table 4, damage voltage is highlighted and is shown by the decrease in RFC and the increase in open-circuit leakage current.

Table 4: GaAs RF switch tested using IEC 61000-4-2.

Vin	Pulse #	I (µA)	I (RFC) (µA)	I (RFC1) (µA)	I (RFC2) (µA)	Open Circuit I (µA)
100V	1x	281	281	281	281	0
	2x	282	282	282	282	0
	5x	281	281	281	281	0
	10x	281	281	281	281	0
	20x	281	281	281	281	0
300V	1x	280	280	280	280	0
	2x	280	280	280	280	0
	5x	279	279	279	279	0
	10x	278	278	278	278	0
	20x	277	277	277	277	0
400v	1x	276	276	276	276	2
	2x	276	276	276	276	4
	5x	277	248	248	248	253
	10x	277	226	226	226	265
	20x	277	214	214	214	268

After the ESD mini-zap tests, the RF switch was re-tested using the TLP system to establish the TLP failure voltage. Table 5 shows TLP testing of the un-protected GaAs switch; TLP testing caused the GaAs switch to fail at 200 V. This was a level 200 V lower than with the ESD gun. Damage onset is highlighted.

Table 5: GaAs RF switch tested using 48 ns TLP tester.

Vin	Times	I (µA)	I (RFC) (µA)	I (RFC1) (µA)	I (RFC2) (µA)	Current w/ open circuit (µA)
100V	1x	263	263	263	263	0
	2x	263	263	263	263	0
	5x	263	263	263	263	0
	10x	263	263	263	263	0
	20x	262	262	262	262	0
200V	1x	262	262	262	262	1
	2x	262	262	262	262	4
	5x	264	158	158	158	261
	10x	263	147	147	147	261

Actual scope traces show the GaAs switch clamp voltage increasing with time when pulsed at and above 200V TLP.

The TLP data of Table 5 indicates the PVS component's trigger voltage for protection of the GaAs RF switch needs to be less than 200V. Based on this data, an 0603 PVS device with a 100 V trigger voltage was selected for ESD protection of the GaAs RF switch. A 200 V PVS was also tested to evaluate the test method. Figure 7 shows the test circuit for the ESD testing. V1 and V2 are ground that turns off the 2 switches. The ESD pulse is applied to the RFC node.

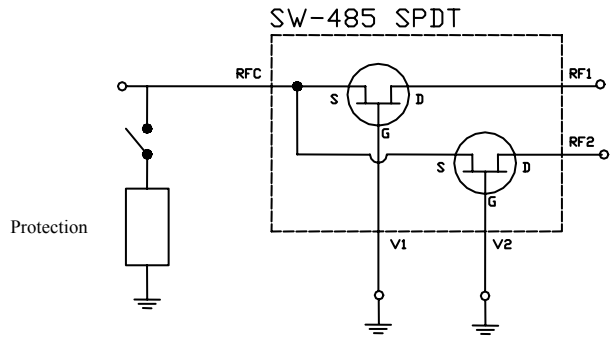

Figure7: Test setup for ESD and TLP testing of RF switch.

The post-ESD pulse setup to verify the condition of the GaAs RF switch is shown in a generic setup in Figure 8. A 3 V DC is applied to V1 turning on switch 1. An ammeter (in series with the power supply) is used to measure the current to ground at $RF_{(C,1,2)}$. If the device is functioning properly, the current I= I(RFC1), I(RFC2), and I(RFC); if the current is less than I then the device has failed. If the open-circuit current exhibits leakage the device has also failed.

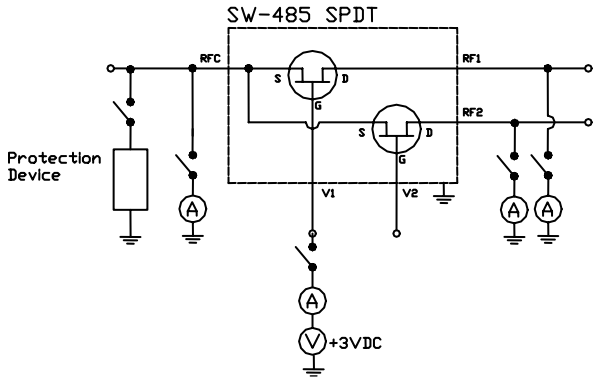

Figure 8: Generic post ESD/TLP test verification of device damage setup.

The actual test platform for the testing, as shown in Figure 9, is a PCB on which is mounted the RF switch and the 0603 PVS device. The PCB allows the RF switch to be replaced repeatedly during the testing.

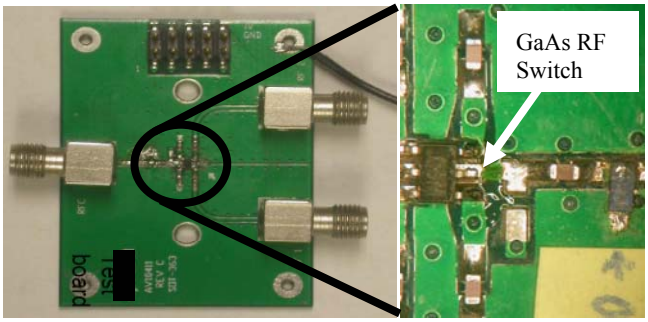

Figure 9: RF switch setup for ESD and TLP testing

VI. System Level Test of Electronics with Integrated PVS Component

After determining the GaAs RF switch failure damage voltage was a 200 V TLP pulse, a 100 Vtrigger 0603 PVS component was soldered on the board in front of the GaAs RF switch; and 8 kV ESD pulses were direct discharged into the circuit using the ESD gun. Voltage levels were initiated at 8 kV, and the device was tested for damage after each 10 pulses. As shown in Table 6, with 100 Vtrigger PVS protection the GaAs RF switch survived over 50 pulses of 8 kV IEC 61000-4-2.

Table 6: GaAs RF switch protected with PVS Surface Mount 0603 tested at 8000 V direct discharge IEC 61000-4-2.

Vin	Times	I (µA)	I(RFC) (µA)	I(RFC1) (µA)	I(RFC2) (µA)
8kV	10x	294	294	294	280
8kV	20x	294	294	294	280
8kV	30x	294	294	294	280
8kV	40x	294	294	294	280
8kV	50x	290	290	290	290
8kV	60x	283	237	237	237
8kV	70x	295	146	146	146

To emphasize the importance of Vtrigger, it should be noted that testing with a 200 V trigger 0603 PVS device did not provide good ESD protection; the RF switch failed on the first 8 kV pulse. In comparison, a 150 V trigger device provided protection for 30 pulses of 8 kV; 10 pulses more than required for conformance to system-level ESD. It was also determined that the 100 V trigger PVS 0603 was not damaged by seventy 8 kV pulses since a new RF switch soldered on the PCB test fixture was also protected by the same 0603.

VII. ESD Device-Level and System-Level Standards of Voltage Suppression Devices

The preceding TLP test protocol with minor or no modification can be used to establish system-level ESD protection using PVS components. As an example, VCSEL diodes were evaluating using a similar protocol. In this case, failure was measured by a 10% decrease in light output of the VCSEL when measured using a photo cell with the device powered. TLP failure was observed at 60 V. Table 7 illustrates the similarity in test protocol to that used for the GaAs RF switch. The 4 and 40 ns data are the voltage response of the VCSEL diode. At a 60 V TLP pulse, the output of the photo-diode dropped from the original output of 332.4 to 254.6 µA. At 70 V input, the photo-diode output dropped by 78% to 74.4µA. To protect this VSCEL, a 50 Vtrigger PVS device that clamped to 23.9 V at 4ns was used to increase survivability to 2 kV HBM.

VCEL # Avg. 5 devices									
Initial Voltage		Current In		Current Out		V4ns		V40ns	
3	V DC only	12.19	mA	332.40	µA	N/A	V	N/A	V
10	V pulse	12.00	mA	324.00	µA	9.33	V	9.69	V
15	V pulse	12.00	mA	324.00	µA	13.27	V	15.02	V
20	V pulse	12.06	mA	326.00	µA	15.52	V	18.76	V
25	V pulse	12.05	mA	326.80	µA	18.56	V	21.46	V
30	V pulse	12.06	mA	326.00	µA	21.01	V	24.20	V
35	V pulse	12.03	mA	325.00	µA	23.12	V	26.19	V
40	V pulse	12.02	mA	324.20	µA	25.06	V	27.39	V
45	V pulse	12.00	mA	324.00	µA	27.36	V	29.76	V
50	V pulse	12.01	mA	322.60	µA	29.17	V	32.46	V
55	V pulse	11.99	mA	304.40	µA	31.85	V	34.52	V
60	V pulse	12.02	mA	254.60	µA	33.69	V	36.49	V
65	V pulse	12.01	mA	149.20	µA	35.56	V	37.88	V
70	V pulse	12.02	mA	74.40	µA	37.50	V	39.23	V
75	V pulse	12.05	mA	34.65	µA	39.37	V	41.29	V

Table 7: VCSEL photo diode current output post TLP testing

Currently, work is in process on protection of a Gigabit Ethernet server. Figures 10 and 11 show that installing a PVS device on a connector pin eliminated most of the 600 V TLP input. In Figure 10, the RJ-45 (with magnetics installed on a PCB on the connector) allows most of the 600 V TLP pulse into the system. The maximum voltage, V_{max}, is 575 V. Figure 11 shows that installation of a 300 Vtrigger device reduces the pulse going into the server by approximately 80% or more, with the majority of the pulse clamped to 36 V. To provide the protection needed the CDE test used by the OEM to simulate voltage discharged by 600 feet of cable will be simulated by a TLP pulse. Simulation will be correlated through pulse current and duration. Once protection Vtrigger is established, a PVS array will be added to the RJ-45 connector.

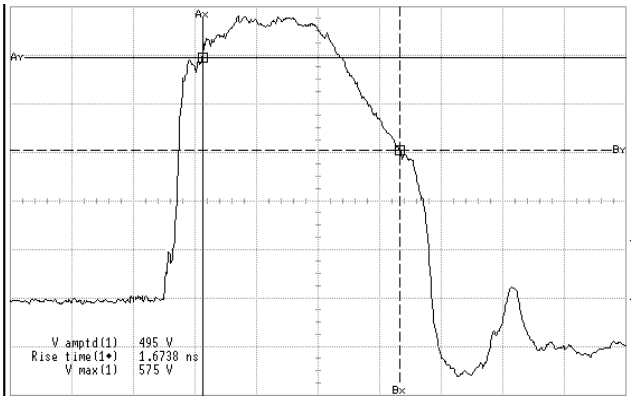

Figure 10: 600V TLP pulse input to RJ-45 connector with magnetics on PCP in the connector

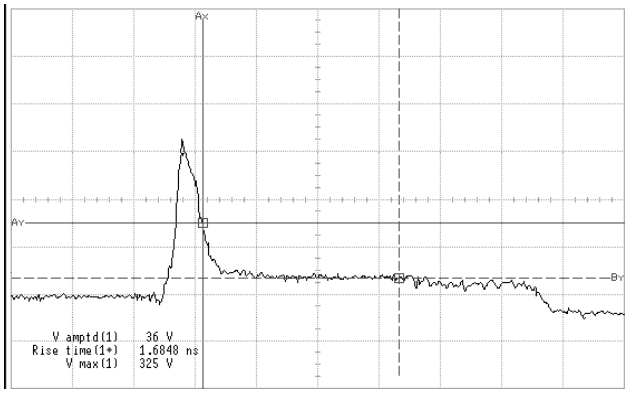

Figure 11: 600 V TLP into PVS protected RJ-45 Connector with magnetics on PCB in the connector

VIII. Discussion

In this paper, a voltage suppressor device made from a polymer was shown to clamp ESD voltages and protect GaAs components from ESD voltages in much the same manner as a traditional ESD diode performs. The significance of the PVS component protecting the GaAs is that it worked where traditional on-chip protection diode structures could not be used because the capacitance loading would interfere with the high speed performance of the GaAs device. Similarly, diodes are not used for protecting a GHz GaAs RF

switch on a PCB because of the capacitance loading. In contrast, the inherently low capacitance of the polymer in the PVS device does not interfere with GHz performance of the GaAs RF switch. There is a strong interest in PVS devices because the low capacitance opens doors for system-level ESD protection of semiconductors and other sensitive components that run at GHz frequencies. Because the polymer film can protect multiple lines at the same time, PVS components also offer manufacturers of electronic boxes and handheld devices a space efficient package for protection of the proliferating numbers of signal lines.

As an example, we have been told a single GaAs RF switch with 8 kV ESD protection can replace 12 pin diodes in a cell phone; and at the same time provide enhanced performance such as video screen at a lower over all cost and using less space. The PVS enables the use of the GaAs RF switch by providing the 8kV ESD protection needed for system level compliance.

In order to provide the ESD protection for the GaAs RF switch it was necessary to do in-house test development to determine the specification needed to protect the GaAs components we tested. Typically, we were informed by the component manufacturer, the GaAs device would survive 20 HBM pulse events of 400 to 700 V magnitudes. To determine how to increase the component survivability to 8 kV system level ESD, we had to use the TLP method and develop correlation procedures between TLP and system level ESD.

The area of development of tests to relate product to system-level events is a whole new research and development area for ESD protection where new standards and methods are needed. Almost every market has a slightly different approach to system-level ESD and a non-common methodology or specification. The TLP method offers a way of bridging the gap between the different cable and other OEM ESD specifications that are emerging. To assure components will survive system-level ESD, there needs to be a test standard that would provide system-level compliance for components assembled on the PCB. Our work with the TLP system has shown a method that may be a procedure that can be used by others in the future.

Presently, TLP Standard Practice (SP) are intentionally focused on on-chip protection and semiconductors. A new standard practice is needed for surge protection devices, board, and system-level issues. We have constantly refined our own TLP method and equipment to achieve correlation between product performance under IEC 61000-4-2 ESD and other cable ESD pulses OEMs are using. By doing so, we are bridging the ESD gap between the component HBM and the system ESD tests to the point where we can show a component manufacturer that the HBM test is inadequate, and a system manufacturer how to design in protection for a component that is not rated for system level ESD. With the increasing use of complex circuits in electronic equipment the need for reliability and uninterrupted performance increases. The sooner new standards emerge the easier it will be to achieve the reliability we all know we have on a land line phone but seldom have on a cell phone.

On more than one occasion, we have observed OEMs that are committed to reliability telling us that they were using a semiconductor from one manufacturer but it was so sensitive and unreliable that they are now using a new manufacturer's chip. By switching to a new chip the problem is usually not solved but the number of field returns is less. System level solutions will be more important as vendors can not achieve adequate results on-chip for the system level demands. New test standards are needed to eliminate field returns.

IX. Future

The use of filled polymer for circuit protection is not new. In the early 1980's, a new polymer fuse that had the capability of re-setting after a current surge was launched in the Telecommunications market by Raychem Corporation. Today polymer positive temperature coefficient (PPTC) devices are used across all electronic markets because of their re-set feature and their ease of construction into low profile films [10]. The low capacitance high-energy ESD sensitive components and semiconductors need is provided by PVS devices.

Additionally, significant work is needed in different packages styles as shown in this paper, such as discrete standard surface mount product protection of GaAs devices, and multiple-array connectors for semiconductors. Once new ESD standards correlating TLP to system-level tests are established, the prediction and verification of PVS devices in system solutions, and their usage will accelerate. It is contemplated that in the future, PVS films can replace the current usage of on-chip protection, opening up new markets, obtaining improved ESD protection for GaAs, magnetic recording industry, and even better ESD results for the 100 to 200 GHz Silicon Germanium heterojunction bipolar technologies [11, 12, 13]. The PVS devices may remove performance barriers for high speed digital GHz technologies, as

well as open the potential for future device technologies.

X. Conclusions

In conclusion, there is a need for new TLP standards to first, correlate components and semiconductors compliance to ESD gun testing per IEC 61000-4-2, and secondly, to expand coverage of system level tests run by OEM to simulate the real world ESD. ESD pulses that take place while connecting long cables to a server port or docking PDA's are system-level ESD tests that are not equivalent to the IEC 61000-4-2 system-level test. We have demonstrated that TLP test procedures designed to measure GaAs component sensitivity can be linked to product performance tests to establish the damage threshold. Then, by using the TLP to characterize PVS devices, we showed that a PVS device, with a turn-on voltage lower than the damage voltage of the GaAs device, increased the GaAs product survivability from 5 pulses at 400 V to over 50 pulses at 8 kV. We are also in the process of determining the same procedures are applicable with modification to alternate applications such as protection of resistors in engine control modules, and semiconductors used in Gigabit Ethernet servers. The introduction of new low capacitance PVS device has forced us to develop new test procedures to help define PVS devices as a solution that can replace ESD diodes.

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References

[1] S. Voldman, "The Impact of Technology Evolution and Scaling on Electrostatic Discharge (ESD) Protection in High Pin Count High Performance Microprocessors," Invited Talk, Proc. of the International Solid State Circuits Conference, Session 21, WA 21.4, 1999, pp. 366-367.

[2] A. Weger, S. Voldman, F. Stellari, P. Song, P. Sanda, and M. McManus, "A Transmission Line Pulse (TLP) – Pico-second Current Analysis (PICA) Tool for Evaluation of ESD and Latchup," Latchup Session, Proc. of the International Reliability Physics Symposium, 2003, pp. 99-104.

[3] R. Troutman, "CMOS Latchup - The Problem and the Cure," Kluwer Publication, 1985.

[4] Palm™ m500 & m505 Cradle Exchange Program, http://www.palmone.com/us/support/m50XUSBcradle.html.

[5] Electrostatic Discharge Association, Fundamentals of ESD, Device Sensitivity and Testing, Part V, http://www.esda.org/basic/part5.cfm.

[6] ESD Association Standard Practice on Electrostatic Discharge Sensitivity Testing: Transmission Line Pulse (TLP) -Component Level, DSP5.5.1-2003

[7] T. Maloney and N. Khuarana, "Transmission Line Pulse Technique for Circuit Modeling and ESD Phenomena," Proceedings of the EOS/ESD Symposium, 1985, pp. 49-54.

[8] Vishay Data Sheet, " Low Capacitance ESD Protection Array for High Speed Data Interfaces", http://www.vishay.com/docs/85806/85806.pdf

[9] Electronic Polymers Inc. Web Site, "EPI FLO Surface Mount and Connector Array ESD Supressors," http://www.electronicpolymers.com

[10] Technical Paper, "Fundamentals of Resettable Functionality in PPTC Devices", web site http://synergy.sager.com/ProductPDFs/re-settable_fuses.pdf.

[11] A. Wallash, T. Hughbanks, and S. Voldman, "ESD Failure Mechanisms in Inductive and Magnetoresistive Recording Heads," Proc. of the EOS/ESD Symposium, 1995, pp. 322-330

[12] C. Richier et al., "Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 GHz) in a 0.18 um CMOS Process," Proc. of the EOS/ESD Symposium, 2000, pp.251-260

[13] S. Voldman et al., "Electrostatic Discharge and High Current Pulse Characterization of Epitaxial Base Silicon Germanium Heterojunction Bipolar Transistors," Proc. of the International Reliability Physics Symposium, 2000, pp.310-316