

EMBEDDING A THIN POLYMER VOLTAGE ESD SUPPRESSING CORE IN A CHIP PACKAGE - ALTERNATIVE TO ON CHIP ESD PROTECTION

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Abstract

Today's portable cell phones and commercial electronics have the potential to impact the quality of our daily lives by the reliability of their performance. One of nature's hidden threats to electronics is electrostatic discharge (ESD). As the electronics content of our daily lives continually expands, we have become more and more dependent on electronics that contain digital chips whose ESD reliability is getting worse. Engineers are being forced to sacrifice reliability for performance in the competitive race to provide more features in less space.

This paper describes the ESD problem and how it has been solved with new nanomaterial filled polymers. It describes how the ESD suppressors are tested and how the new material enables designers to design in protection in the packaging.

A cell phone is used as a well known example of a device which has ESD sensitive I/O channels. EPI's surface mount technology and EPI-Core embedded in an IC package can be applied as an easy and cost effective way to attain ESD protection.

Key words: ESD-protection, embedded passives, reliability testing

Introduction

The drive for new features has been supported by advances to 65nm CMOS chips and GaAs chips which are far more sensitive to ESD than their predecessors of 5 years ago. In 2005 the National ESD Association published a roadmap showing ESD sensitivity of CMOS chips has not only taken a huge nose dive over the last five years, but also the map is predicting ESD sensitivity is going to get even worse between now and 2010. [1] ESD survivability in 1995 for Human Body Model (HBM) ESD was at 2000 V, today, in 2006 HBM survivability has dropped to 200V, and is heading to less than 200V.

Further exasperating the ESD problem is the trend towards pervasive use of portable electronics, which led to the introduction in early 2000 of a system level ESD standard that anticipates the amount of current a digital chip can be exposed to at the system level is going to increase from HBM, worst cast, of ~ 6 Amps to System Level Current of ~ 30 Amps. The duration of the ESD event is extremely short, typically less than 100 ns, but the speed of System Level ESD is so fast that it can reach 8KV in 1 ns. In 2002 Scientific American

published an article written by an IBM expert of on-chip ESD design stating "Electrostatic discharges threaten to halt further shrinking and acceleration of electronic devices in the future" indicating ESD protection on semiconductor components is a barrier to Moores Law. [2] The key problem is digital chip designers need low capacitance ESD protection structures on chips in order to run at high frequencies without interfering with the signal transmission. Since no cost effective solution has been readily available to the ESD Engineer, the only alternative has been to trade reliability for performance. It is estimated that 27-33% of customer returns are due to ESD returns. [3]

Polymer voltage suppressors

At Electronic Polymers Inc., EPI, we have developed EPI-FLO™ ESD polymer voltage suppressors specifically for ESD protection of sensitive digital chips. Initial product developed was standard foot print 0402 Surface Mount components for protection of IC's from HBM and System Level ESD. The Surface Mount product led to EPI-FLO™ Connector press fit arrays capable of multiple line ESD protection.

The EPI-FLO™ polymer is manufactured as laminate 12x18” sheets, with the voltage sensing polymer sandwiched between copper sheets. The typical sheet thickness is less than 2 mils, composed of .75 mil copper. Using standard printed

circuit board circuitizing processes the laminate is transformed into EPI-FLO™ Surface Mount and Connector Arrays devices. **Figure 1** is a cross sectional diagram of an EPI-FLO™ Surface Mount

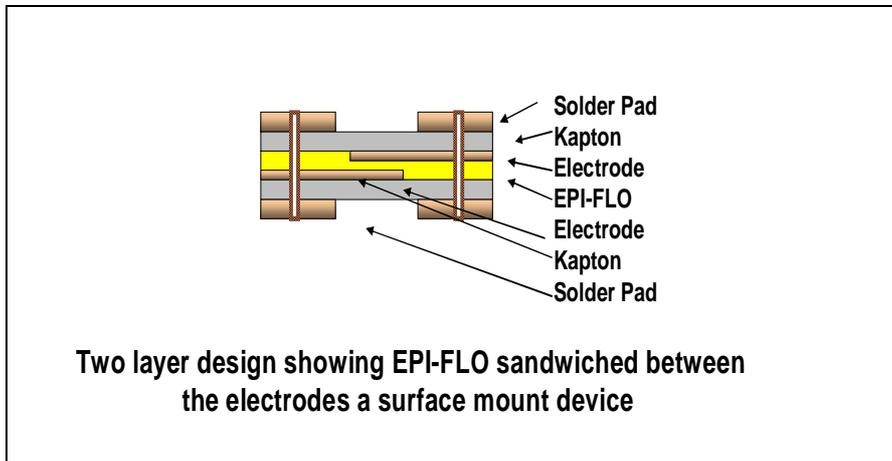


Figure 1: EPI-FLO™ is between the two electrodes of the surface mount device.

EPI has also developed product design to accommodate the build of a 4 layer package with embedded EPI-FLO™. Specifically, EPI has designed a method to embed EPI-FLO™ in the package of a cell phone GaAs power amplifier. This design involves extending the through hole via process and etch process that EPI used previously for two layer Surface Mount and Connector Array devices. **Figure 2** is a diagram of the etched EPI-FLO™ laminate embedded in a 4 layer Power Amplifier board. Table 1 list typical SMT data sheet parameters. The unique feature of the SMT that leads to the concept of embedding EPI-Core™

in IC Packages is the fact that there EPI-Core material is the substrate combining the ESD voltage suppression with the Femto Farad capacitance of EPI-Core™, opens the door for off chip ESD suppression in the IC package. EPI-Core™ embedded in the package provides I/O as well as pin to pin protection in cooperation of EPI-Core™ laminate in an IC package adds another layer in the package board, transforming a 2-layer into a 4 layer board. The EPI-Core™ increased the package thickness by 2 mils (mm)

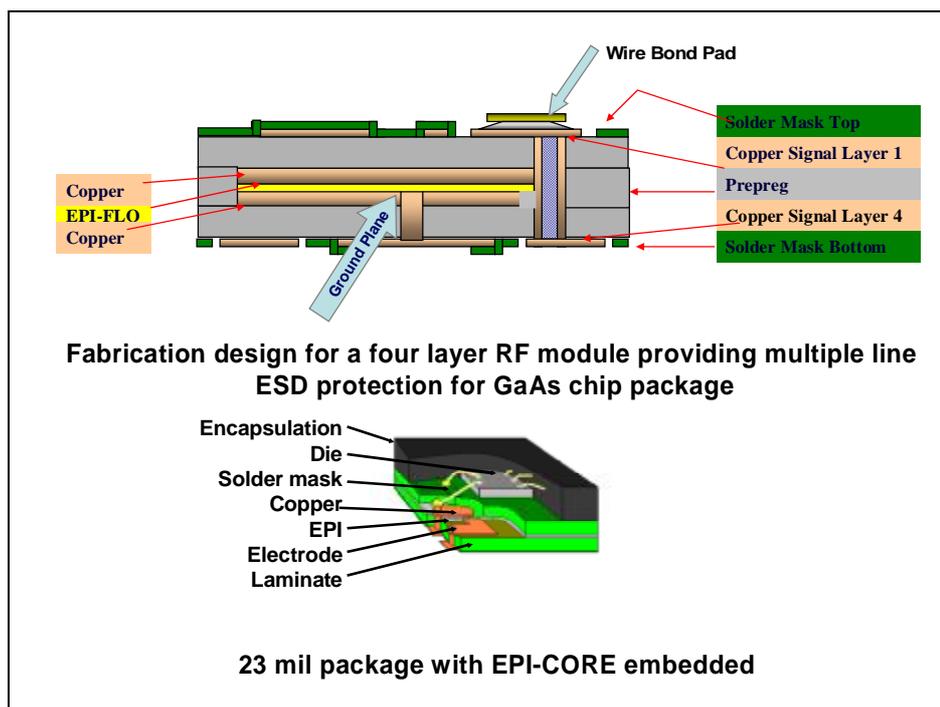


Figure 2: EPI-CORE can be embedded in semiconductor packaging.

EPI also designs press connector arrays for USB & Ethernet connectors (RJ-connector). Recent work with processor manufacturers include BGA and PGA packages including a full EPI matrix. **Figure 3** shows an EPI-FLO™ connector array that has been press fitted onto a microprocessor chip for prototype evaluation prior to building EPI- Core™



Figure 3: EPI-FLO™ connector array is made to be press fitted onto microprocessor chip.

into the package from the EPI- Core™ laminate. The artwork for connector array allows for direct attachment of ground pins to the array ground with a press pin fit design. Similarly sensitive signal pins use a press fit to washer, to provide an electrode for shunting ESD pulse to ground.

Cell phones ESD sensitivity and protection

All electronic devices are ESD sensitive on their I/O channels. In a mobile phone these are antennas, keyboard and microprocessor. In addition to protecting the I/Os, components next to the I/O must also be protected. Such components include the PA and the LNA. These are the components may be degraded or killed by the ESD pulses. Phone operators report identifying a large number of dropped calls caused by ESD degraded components, especially PAs. Thus ESD protection

is a common interest for all in the supply chain, the operator and the user.

Protection of the antenna and human interfaces is fairly easy, but it needs a holistic approach, independent of component suppliers. **Figure 4** details the most ESD sensitive components of a high end mobile phone. To reap the benefits of reduced weight, space, height and reliability of a cell phone requires design work during the cell phone design phase.

Areas detailing the use of SMT, connector, and EPI- Core™ embedded in the package are shown in Red.

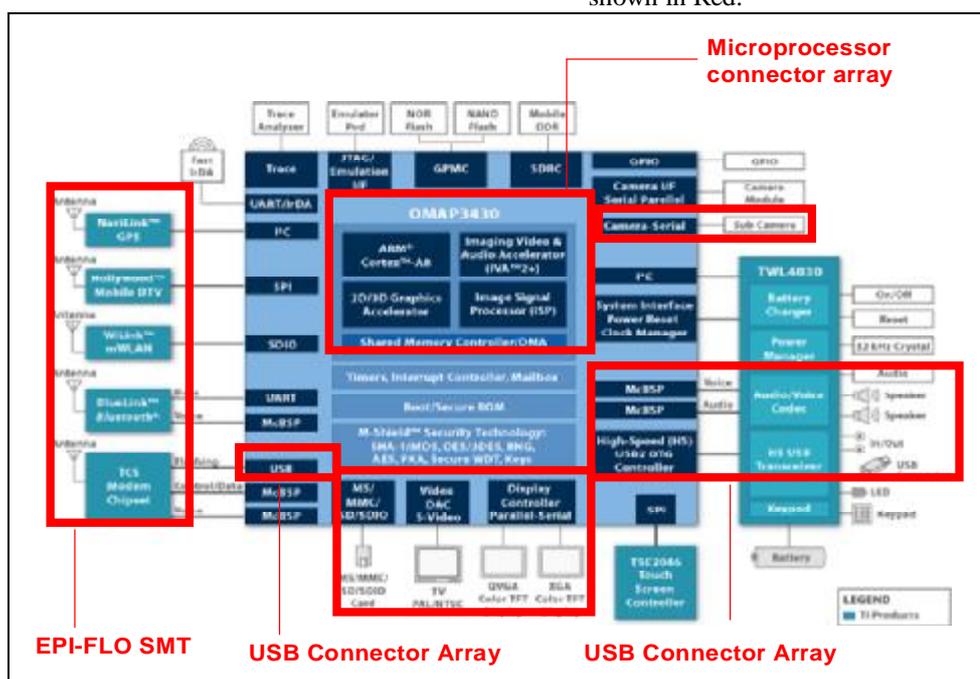


Figure 4: ESD sensitive areas of a mobile phone are outlined in red as well as EPI-FLO™ protective solutions.

Test protocols for ESD protection of chips

At Electronic Polymers test protocols and test equipment have been developed to enable ESD protection of sensitive chips. We have used our test protocol successfully to protect chips from Human Body Model, Machine Model, Charged Device Model, System Level IEC 61000-4-2, and the new Cable Discharge Event ESD. To provide ESD solutions we first determine the failure voltage of the chip using the ESD standard specified, and then using our System Level/IC, Very Fast Transmission Line Pulser with a 126Hz, 40Giga samples/sec sampling, 1.5, 18 GHz rate, we establish the voltage and current that damages the chip. The EPI-FLO™ is then specified to turn on at a lower voltage. Then the IC fails to dissipate current which would cause IC failure. The protection is verified initially by building test fixtures and mounting EPI-FLO™ surface mount 0402 units in front of the pins to be protected. Protection is demonstrated by showing the chip can survive multiple ESD hits as required by the specification with both positive and negative pulses. Typically devices are most sensitive to negative pulses. Failure of the chip is measured by a 10- 20% change in leakage current under power. Most PAs will continue to increase the leakage current from μA to milliamps long after the 20% change in leakage has occurred. It is the damaged unit that can cause dropped calls, and increased battery use.

Figure 5 Shows a typical Test setup for a USB VI/IVL curve trace system.



Figure 5 shows a typical test set up

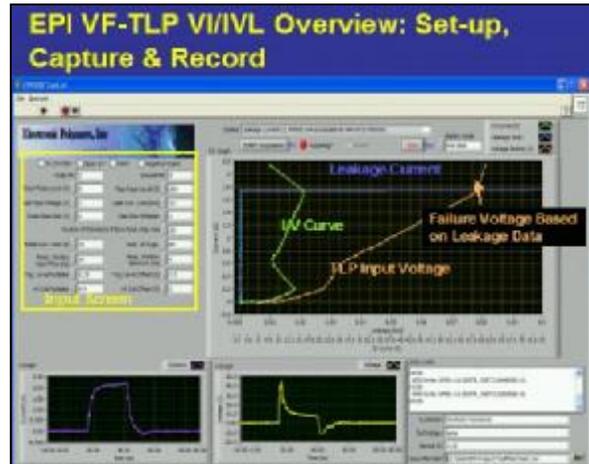


Figure 6: Test set-up panel

Figure 6 shows a VI/IVL curve trace test set-up panel showing input window and cumulative test results from subsequent test pulses.. This system is instrumental in EPI’s failure analysis studies.

Once failure specification is determined, artwork is created for the multi-layer package with ESD protection. The unique benefit of embedding the EPI-FLO directly in the package is multiple protection of signal pins as well as pin-to-pin combinations. As an example, in a 6 pin GaAs power amplifier, 6 pins and 21 pin combinations are ESD protected.

Following is data showing the EPI-FLO enhanced ESD survivability of a GaAs cell phone Power Amplifier to System Level ESD.

Protection of IC

Figure 7 is I/V trace of a cell phone USB IC protected with an 0402 surface mount device, in parallel to ground. The scope trace shows no change in leakage current with 680V and 25.5Amp in the IC. Without EPI-FLO™ protection the device failed at 11 Amps, 440 Volts. To view the current through the chip a current probe was attached to the IC input. To view the current through the chip a current probe was attached to the IC input.

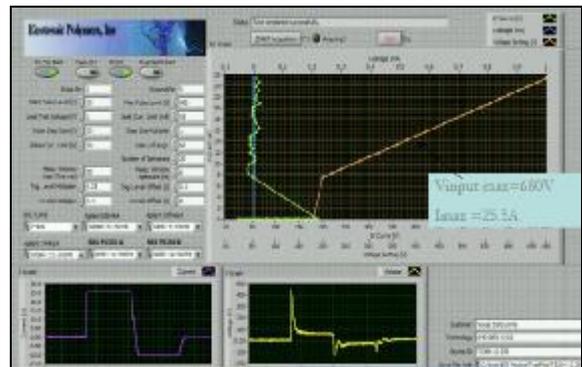


Figure 7: 0402 protection of USB IC to 23Amp.

Figure 8: Below shows the majority of the current goes through the EPI-FLO™. The scope trace shows that with 610 Volts input, 21Amps went through the 0402 and only 1.9Amps went through the USB IC.

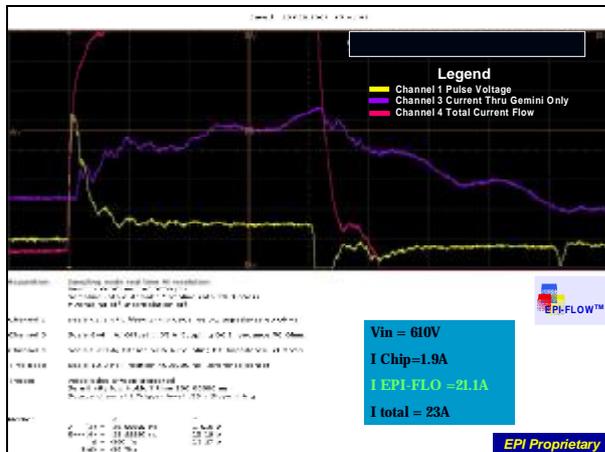


Figure 8: Scope trace shows total current flow on Channel 4, and flow through the IC only on Channel 3, channel 1 is the pulse voltage

Protection of Ethernet Chip

Like the EPI-FLO™ surface mount, the EPI-Core embedded solution has also show protection of Pas. Figure 9 is a typical I/V trace of the protection of the PA with an EPI-Core embedded package. The PA is able to withstand >9A, 250V with EPI-Core. 9Amps correlates to an 8KV HBM ESD, W/O EPI the PA fails at 500V HBM, and 1.5A, 85V on the VI/IVL TLP.

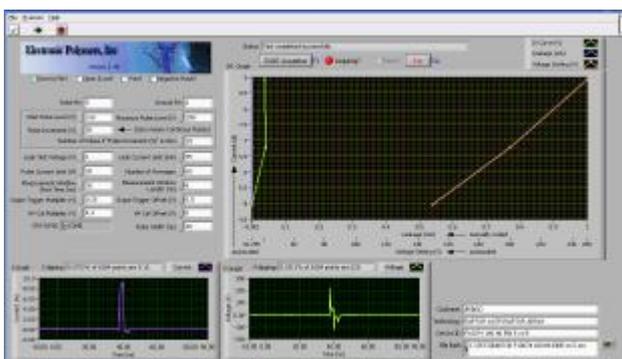


Figure 9: Failure of PA protected with EPI-FLO™ in package increased from 1.5A to > 9A

As shown in the picture, the EPI-FLO™ SMT shunts 21A of current. Therefore, the Ethernet chip is exposed to only 1.9A, and protected from this ESD event.

Conclusions

The reliability of electronic components has been in decline for the last five years. Due to the higher sensitivity and the increasingly small dimensions of electronic components, the risk of ESD damage will only become worse. There are very fast switching protective devices which can protect almost any electronic component. However, most ESD protective components have a detrimental impact on high speed performance and interfere with operating signal.

EPI-FLO™ ESD polymer voltage suppressors have low capacitance, and provide ESD protection without interfering with the IC's operating signal. Further, EPI's various test protocols have provided a means to test certain types of components with different circuitry and environments. It is important to match actual use to specific situations. As a result of testing, EPI has been able to develop EPI-FLO™ polymer voltage suppressors shown to provide adequate as well as cost effective solutions to ESD sensitive devices.

References

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