Cell Phone GaAs Power Amplifiers: ESD, TLP, and PVS Devices

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Abstract: Voltage suppression devices are needed in electronic systems to prevent damage to electrical components from electrostatic discharge (ESD) events. Transmission line pulse testing of GaAs dual mode power amplifiers to determine ESD threshold damage voltages demonstrates the importance of polymer voltage-suppressor device trigger and clamping voltage for module ESD protection.

I. Introduction

With the trend towards smaller semiconductor chip geometries, high frequencies, and the escalating number of signal lines, system level damage of products from ESD has increased due to the shear number of signal lines and the use of increasingly sensitive semiconductors. In the early 2000's the need for system level ESD standards as well as manufacturing ESD standards was recognized with the publication of the IEC 6-1004-2 system level ESD standard. Today even more severe system level ESD standards are emerging to assure the reliability of the proliferating numbers of electronics systems. Cable ESD and Latch-up ESD for handhelds, servers and automotive electronics are known threats to reliability and are recognized as needed new specifications. Transmission Line Pulse (TLP) standards are being proposed to provide test protocols for multiple ESD standards [1, 2, 3, 4].

Recently the ESDA association published an ESD Technology Road Map that shows CMOS semiconductor ESD survivability is being sacrificed for performance [5]. Between 1995 and 2005 the level of ESD protection on CMOS IC's has been reduced from a minimum of 2000V Human Body Model HBM to 200V. The trend for reduced CMOS ESD protection is so strong that in 2005 minimum Charged Device Model (CDM) and Machine Model (MM) ESD has dropped to less than 200V. Figure 1 shows an approximately 50% reduction in ESD standards protection level every 5 years.

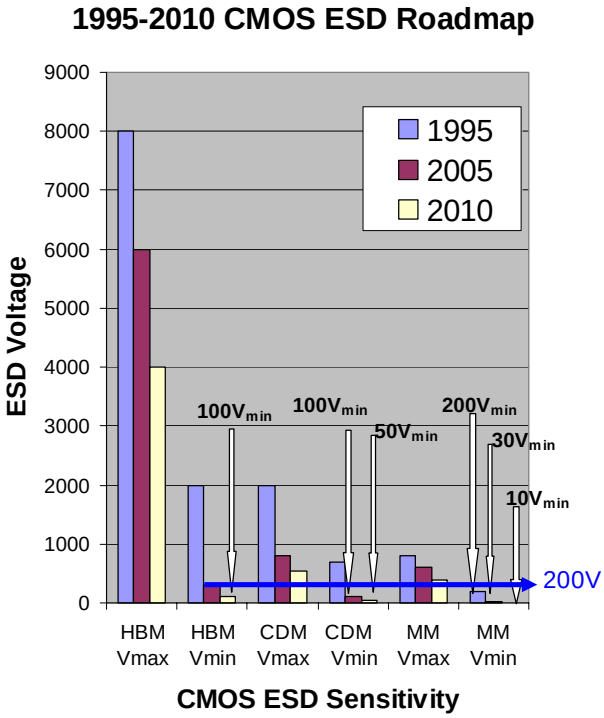

Figure 1: The National ESDA Technology Road Map shows engineers are sacrificing ESD reliability for performance

The reduction in ESD protection is being driven by lower capacitance budgets needed for GHz frequencies and by reduction in space available for ESD structures on both semiconductors and printed circuit boards. The ESD Roadmap clearly shows a need for new ESD solutions.

To assist in solving the ESD problem the TLP is emerging as a tool that bridges the gap between system level ESD and IC level ESD. In Figure 2 below, the chart of the current in various ESD Standards plotted against TLP voltages links on a single chart 3 ESD standards. The current versus voltage trace for the HBM and the IEC system level using TLP as the correlation tester shows the system level specification for 8000V ESD is 24A versus only 1.3A for 2000V HBM ESD. While chip designers are reducing ESD protection structures to gain performance, creeping up on the system side are new and more severe ESD standards to deal with increased handling of electronic systems by the end user.

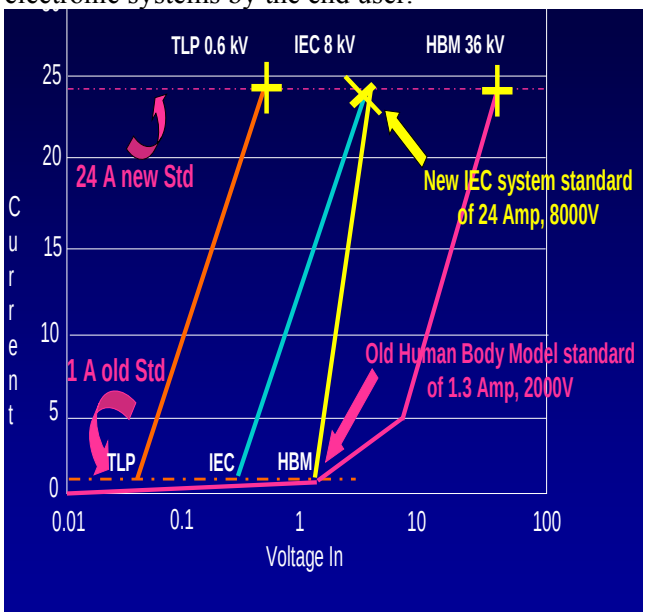

Figure 2: TLP testers and test protocols bridge the gap between system and semiconductor ESD standards

Adding to the ESD dilemma on the system side of the equation is the technology focus towards removing components from the printed circuit board. The directive from the National Electronics Manufacturing Initiative (NEMI) is to remove 40% of passive components from the printed circuit board by 2008. The NEMI Technology Roadmap focuses on embedding passive components in printed circuit boards to reduce the number of components on the board thereby reducing costs, saving space and enhancing performance [6].

ESD protection for all signal lines in both hand held and fixed electronics is emerging as a major need for improving product reliability and mean time before failure (MTBF), both of which can impact a company's profitability through customer dissatisfaction and field returns. Hand held devices such as PDA's, cell phones, and fixed electronic systems such as computers, and servers are constantly exposed to system level ESD during handling and information transfer processes such as docking. Equipment end users do not want to re-boot cell phones or computers, or worse yet, loose data and time as a result of component damage or latch-up caused by a system level ESD pulse [7].

An emerging solution for improving ESD protection is low capacitance polymer voltage suppression (PVS) surface mount devices, connector arrays and embedded structures. Since capacitance degrades high speed signals, the lower the capacitance of an ESD protection component the better. Today's GHz signals need the femto farad capacitance available in PVS devices. The low dielectric constant of the polymer in the PVS device inherently provides capacitances that are less than 200 fF. Silicon diodes and other traditional ESD protection devices such as surface mount capacitors have higher dielectric constants than PVS devices and as a result their capacitances tend to be in much greater, in the pF range [8, 9].

In addition to providing fF capacitance, the polymer in PVS components is also inherently suitable for designing space efficient packages such as multiple array ESD surface mount devices, ESD connector arrays (Figure 3), and embedded ESD layers in integrated circuit packages.

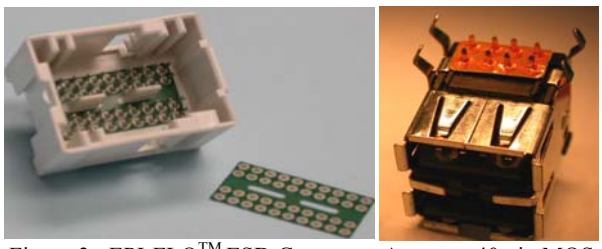

Figure 3: EPI-FLO™ ESD Connector Array on 40 pin MQS automotive engine control module connector and a RJ-45.

Due to the low capacitance, PVS devices can be used for semiconductor HBM, MM, and CDM specifications. It is also ideal for IEC 6-1004-2 system level ESD protection in GHz RF

applications such as GaAs cell phone modules [10]. The low capacitance of the PVS device is ideal for ESD protection of RF frequencies. The GaAs dual mode GSM/PCS power amplifier discussed in this paper has no built in ESD protection structures and consequently is very ESD sensitive.

The manufacture and specification of PVS surface mount components and connector arrays has required the development of TLP test equipment and TLP ESD test procedures for correlation of PVS device trigger voltage performance to the ESD failure voltage of the device to be protected. The ESD standards vary depending on the application. Typical standards to correlate TLP to are MM, HBM and IEC 61000-4-2 ESD standards. More and more frequently, both MM and HBM or CDM and HBM are required, with the ultimate goal being the IEC specification.

To provide protection for semiconductors using PVS devices we determine the ESD and TLP voltages that damage the semiconductor. Damage is typically defined as an increase in leakage current when the device is powered after being pulsed. Typically the HBM failure voltage is already well known by the user and this is information is used to calculate the HBM failure current. From the damage current the TLP damage voltage is estimates using the chart of Figure 2.

Using our test procedure, the semiconductor device under test (DUT) is pulsed with a specified number of TLP pulses per voltage level, typically between 3 and 20 pulses positive and negative, depending on the ESD standard specified. Next, a PVS device with a lower TLP turn on voltage (Vtrigger) than the TLP damage voltage of the DUT is positioned in the circuit in front of the DUT. To demonstrate PVS protection, the DUT is next tested using the ESD standard called out for the application. Using this TLP test protocol a GaAs component that failed 450V IEC doubled its ESD resistance with a 150V PVS 0402 surface mount device.

This TLP test procedure combine testing practices used for the design of ESD structures on IC's [11] with TLP test methods that correlate to the pulse delivered by an ESD Standard. This paper describes the TLP equipment and test procedures used to improve a dual mode power module amplifier's HBM ESD damage threshold by incorporating a PVS device with a Vtrigger below the TLP damage threshold of the module lines.

II. System RF/ESD Compliance Procedure and Equipment

A tri-band power amplifier module for use in cellular telephone handsets was used in this study. It contains two GaAs integrated circuits (ICs) based on the enhancement-mode pseudomorphic high-electron mobility transistor (E-pHEMT) technology, both of which are manufactured by Agilent. The dual mode integrated circuits work in the GSM band around 800 to 900 MHz and the DCS and PCS bands around 1700 to 1900 MHz. Both the GSM line and PCS/DCS line with sites for soldering the PVS devices on a demo board are shown in Figures 4 and 5.

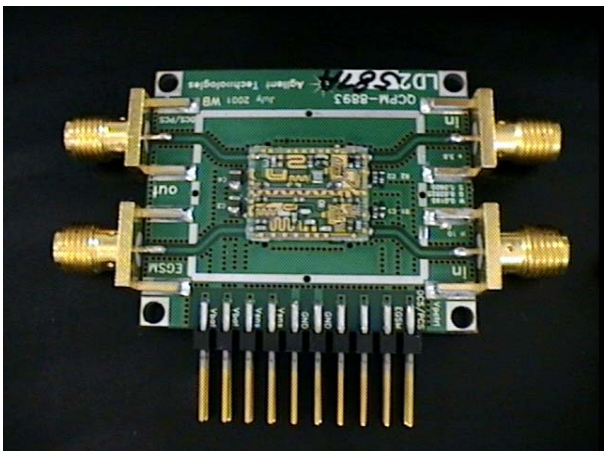

Figure 4: Demo board for Dual GSM and PCS/DCS module

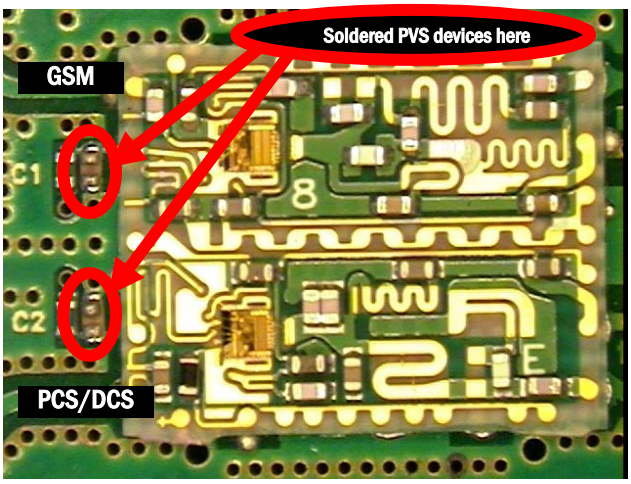

Figure 5: Dual GSM and PCS/DCS module site for soldering surface mount 0402 PVS ESD protection device

Test measurements were performed using an EPI 50 ohm TLP system with a 200-300 ps rise time, a HBM ESD gun and a HBM IC tester. The first step was to characterize the GSM and the PCS/DCS power amplifier modules prior to HBM or TLP testing. The RF performance and the I-V performance from 0 to 2.5V were measured. The PVS device used was an EPI surface mount device as show in Figure 6.

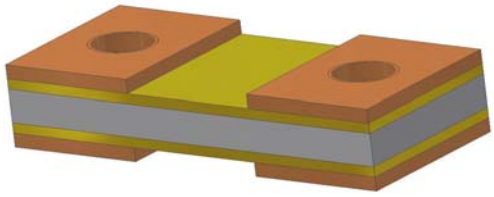

Figure 6: PVS Construction for 0603, 0402, 0201 Electronic Polymers Inc. EPI-FLO™

III. Measurement of PVS Device Impact on RF Performance

RF performance of the power amplifier module was measured with and without the low capacitance 0402 surface mount PVS ESD protection component. RF was also measured on a .5pF capacitor for comparison to the capacitance of the PVS surface mount device. As shown in table 1 the capacitance of the device did not interfere with RF performance. The power module performance with the PVS device exceeded the module performance with a .5 pF capacitor.

Table 1: RF of GSM control versus GSM with PVS 0402 device and GSM with a 0.5pF capacitor on the RF out line

	GSM Control	150Vt PVS 0402	0.5 pF capacitor
GSM Freq (MHz)	Power output (dBm)	Power output (dBm)	Power output (dBm)
824	34.35	34.32	34.5
836	34.66	34.66	34.73
849	34.78	34.82	34.82
880	35.08	34.91	34.95
900	35.07	34.87	34.73
915	35.01	34.81	34.67
Power output comparison versus control			
Best performance		+0.04dbm	+0.07dbm
Worst performance		-0.2dbm	-0.34dbm

The RF degradation (power output at full power setting) appears to be purely a tuning effect due to the 0402 surface mount PVS ESD protection components' capacitor-like behavior. The capacitance on the 0402 devices is <200 fF based on LCR measurement. The design of power amplifier can incorporate the ~200 fF parasitic capacitance as part of the compensation circuit. If designed and accounted correctly, a broadband match (Return Loss <-15dB) at least up to 10GHz with PVS ESD protection can be demonstrated.

IV. TLP and HBM Testing of GaAs Power Amplifier Modules with and without PVS in the Circuit

GaAs power amplifier samples built with and without PVS component were subjected to HBM ESD pulses using an IMCS system 700 ESD tester. As typical in the industry, three consecutive pulses were applied as per the JDEC HBM specification. Samples were tested by applying a broad range of voltages below and above the ESD threshold, each voltage was pulsed once under both reverse and forward bias conditions. In all cases, the devices were characterized by IV and visual inspection before and after the ESD pulsing.

During testing damage three signatures were observed to be characteristic of ESD damage and failure. First, after damage, the RF power output degradation drift was more than 1 dBm. Second, the leakage current increased from micro amps to milli amps and, third, the characteristic control voltage (Vapc) at full power drifted by more than 20%. The ESD withstand voltage and time to failure for the module was consistent.

Changes in the leakage current and power degradation are observed immediately after the intentional ESD damage. On pulsing with damage threshold ESD pulses, the leakage current when powered at voltages less than 2 Volts increases. Once a device is pulsed above the ESD damage voltage threshold, degradation tends to set in rather quickly. In Figures 7 and 8 respectively, the comparison of the degradation of the PCS/DCS line leakage current after testing and power setting as a function of ESD test levels between units without PVS (control) and units with PVS is shown.

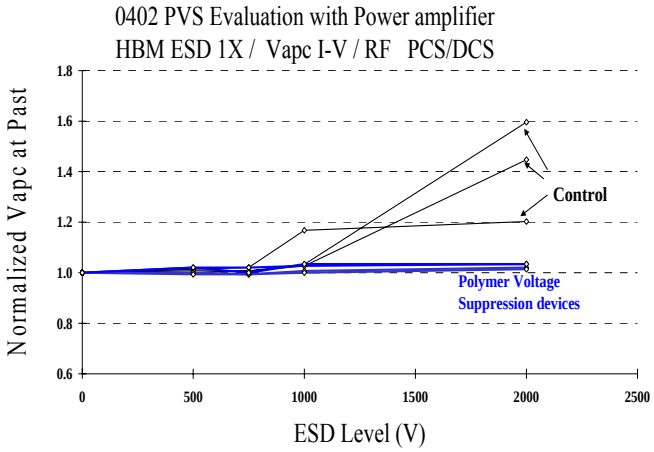

Figure 7: Device power setting degradation takes place at significantly lower ESD voltages without PVS protection.

Depending on the exact stress conditions, ESD pulses will in many cases lead to an increase of the current threshold and power degradation, as demonstrated in Figures 7 and 8. These changes are significant enough to demonstrate the ESD enhancement of power amplifiers with PVS devices. It is therefore proposed that monitoring the change in leakage current and power settings offers a very effective way to screen for latent ESD damage. Figure 8 shows that devices that have been zapped with ESD voltages at or above the ESD voltage threshold will degrade in leakage current output by more than 20%. Figure 8 shows that devices that have been zapped with ESD voltages at or above the ESD voltage threshold will degrade in leakage current output by more than 20%.

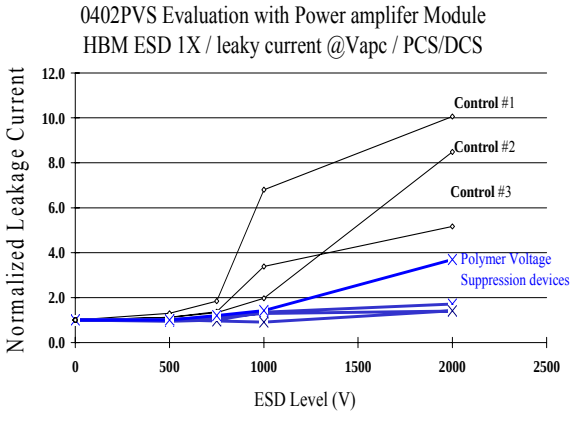

Figure 8: GaAs leakage degradation increases significantly at lower ESD voltages without PVS protection

Table 2 summarizes the failure rate as a function of HBM ESD levels found for the power amplifier with and without PVS. At first glance, it is striking that the units with PVS have generally much higher ESD damage thresholds than all control devices (2000V vs. 1000V HBM). For the control units without PVS devices after HBM ESD zaps of 750-1000V, significant changes in the power setting parameters and leakage current become visible.

Table 2. ESD damage thresholds of GaAs with/without PVS.

Units Tested	Time 0	Full Power	Control Voltage @ full power	Forward Leakage Current	Life with PVS
Control	**ESD Level**	**Psat (dbm)**	**Vapc (V) @ Pset**	**I@ 0.5V @Vapc**	
3 ea	**500V**	3/3 Pass	3/3 Pass	3/3 Pass	
	750V	**2/3 Pass**	3/3 Pass	**2/3 Pass**	
	1000V	**0/3 Pass**	**2/3 Pass**	**0/3 Pass**	
	2000V	**0/3 Pass**	**2/ 3 Pass**	**0/3 Pass**	
PVS	**ESD Level**				
4ea	**500V**	4/4 Pass	4/4 Pass	4/4 Pass	Same
	750V	4/4 Pass	4/4 Pass	4/4 Pass	Better
	1000V	4/4 Pass	4/4 Pass	4/4 Pass	Better
	2000V	**3/4 Pass**	**3/4 Pass**	**1/4 Pass**	Better
Failure criteria:		drift> -1 Dbm	drift >20 %	drift >20%	

The ESD damage effects are most noticeable with leakage current measurements. The units with PVS survive 1000V and show only minor degradation even at 2000V.

The TLP testing was carried out on sister devices to the devices tested with the HBM testers. The TLP procedure used was more aggressive than the HBM testing since TLP testing was a new means of testing the power amplifier modules. For HBM 1 pulse positive and 1 negative pulse was used. For TLP the sequence was 5 pulses positive and 5 pulses negative. The TLP pulse applied to the device was 48ns in width. Testing started at 20V and increased using a defined step stress of 10 to 20V. Traces were recorded after 3X+, and 3X− and leakage current at 1.5 V was recorded after each pulse. A 20% change in the current after pulsing

was set as device failure. Testing was stopped after device failure increased from µA to mA.

The TLP Voltage-Time characteristics are a series of single pulse events in which each I-V point represents the recorded current and voltage across the DUT during a pulse test event within the measurement window. The TLP is a highly sensitive and repeatable method employed in the IC industry to identify IC failure voltage threshold. Here, the method was used to see characteristic changes in the TLP trace response as a possible fingerprint of the ESD failure mode of the GaAs power amplifier module. In figures 9 and 10 the device is not damaged by the TLP pulse and leakage is µA.

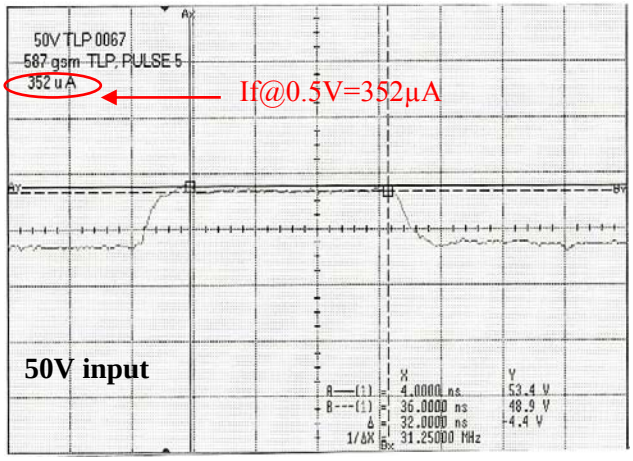

Figure 9: Scope trace for 50V TLP pulse into GaAs Module shows no damage to the device

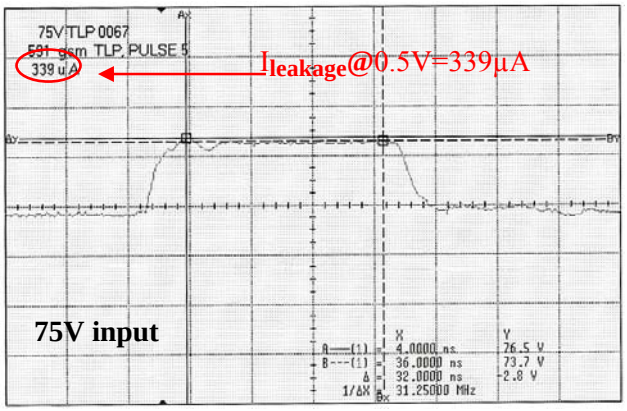

Figure 10: Scope trace for 75V TLP pulse into GaAs module shows no damage to the device

Careful visual observation of the charts in Figure 10 and 11 indicates failure of the modules at an 85V TLP pulse. Significant visible changes typically occur in the center portion of the trace. The changes in the center of the scope trace are believed to be the damage signature created by the ESD pulses. Beyond or at the TLP damage threshold levels, the trace shows a distortion that contrast noticeably with the original square trace observed below the voltage damage threshold. The change in the voltage on the trace is a result of impedance changes within the DUT. Under high TLP bias input conditions, these damage spots within the DUT circuit provide leakage paths and lead to a localized disturbance to the TLP output traces as shown in Figures 11, and 12.

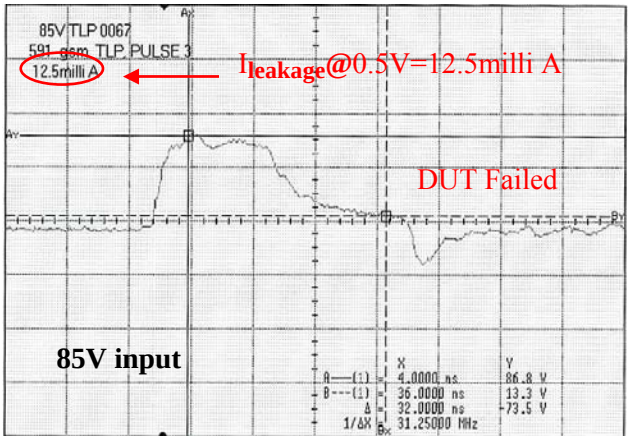

Figure11: 85V TLP pulse in GaAs module damaged module

In Figure 12 a 100V TLP pulse increased leakage from 12.5 milli A to 32.9 milli A.

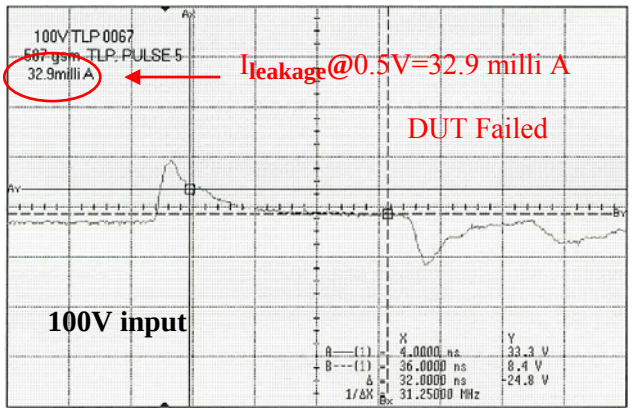

Figure 12: 100V TLP pulse into GaAs module increase damage to module

For devices ESD stressed above the ESD voltage threshold a darkening of areas of the DUT was observed, as shown in Figure 13. The damage region was identified as the melting point of 2K ohm resistor of 6 micron width within the MMIC.

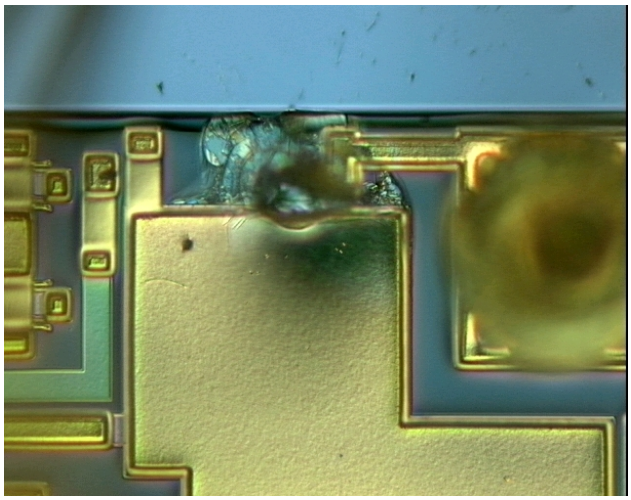

Figure 13: TLP Testing of GPS mode to failure shows visible damage on the device circuit

V. Leakage Current as a Measure of Device Damage

For the purpose of this study, changes in the leakage current have been taken as an indication for ESD-induced damage. For the various device types (GSM vs. PCS), testing models and stepwise stress conditions, the ESD voltage threshold has been defined as the voltage leading to onset of change in the leakage current. The TLP data indicated the GSM damage threshold was 85V and the PCS was 125V TLP, as shown in Figure 14.

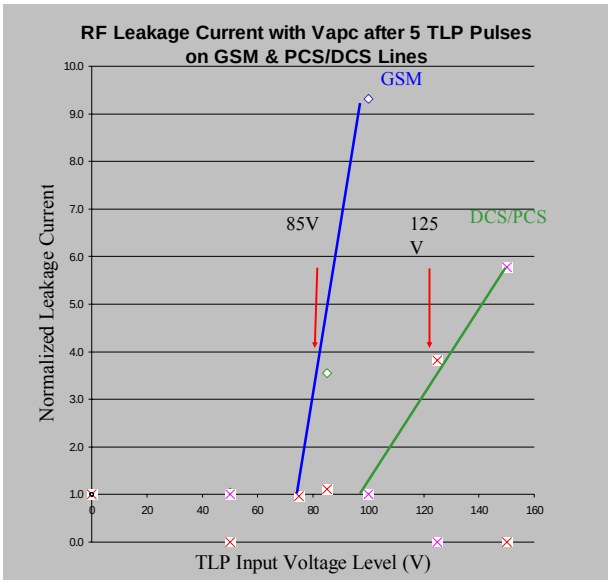

Figure 14: TLP damage threshold degradation curves from leakage current measurements at 1.5V

Incorporation of a 150V PVS 0603 surface mount device on the less sensitive PC/DCS mode increased ESD survival from 500V HBM to 900V HBM (Figure 15). To increase survival to 2000V requires a PVS device with a trigger voltage less than 125V. To achieve system level IEC ESD a PVS with < 100V trigger voltage and a low clamp voltage is needed.

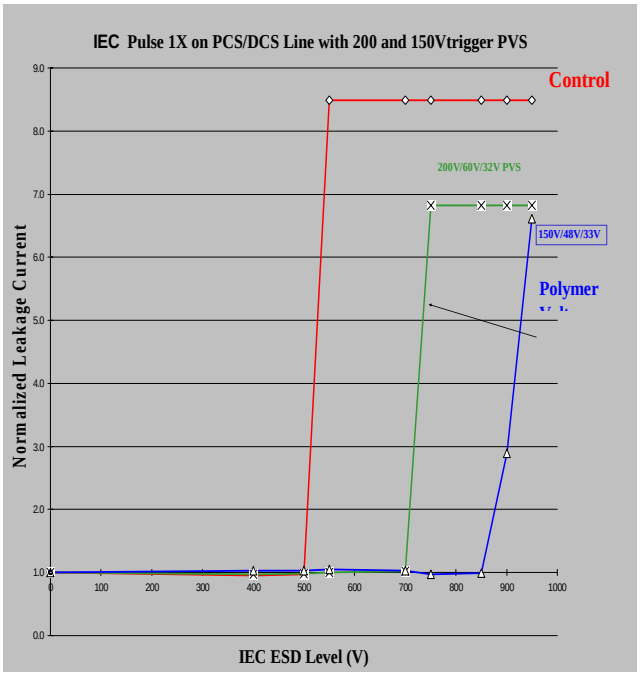

Figure 15: HBM testing of PCS/DCS module with 200V and 150V PCS device show ESD protection increases by 2x with 150V PVS device

VI. Discussion

The work done on the dual mode power module protected by a Surface Mount PVS device opens doors to allowing devices such as GaAs which have no ESD protection on the die to survive to levels of 2000V HBM and exceed the JDEC JESD22-C101C 500V Specification. This is a factory level specification. By lowering the voltage turn on of the PVS device the ESD survivability of sensitive IC's can be extended to system level IEC 6-1004-2 ESD, thereby providing the potential for both factory and user ESD reliability.

For the dual mode power module amplifier tested the difference in ESD susceptibility between the GMS and the DCS/PCS line was unanticipated. The sensitivity of the GMS line had not been

observed during HBM testing. To protect both lines on the module requires a PVS device with a Vtrig of 125V on PCS/DCS line. The GMS line needs a Vtrigger of approximately 85V. Using the 150V and the 200V PVS device HBM survivability was achieved. To achieve IEC system level ESD the lower trigger voltages are required.

The advantage of the TLP test method over the HBM test procedure was to clearly distinguish the ESD performance difference between the GSM and the DCS/PCS line. Also, the signature of the TLP traces clearly correlated to leakage current damage and to the reduced power output of the amplifiers. Using the TLP rather than the ESD HBM tester to provide the damage threshold for the GaAs power module amplifiers provided more accurate information making the damage threshold information more easily obtained and understood.

VII. Future

PVS devices are a new technology for increasing the ESD performance and therefore the reliability of both integrated circuits and electronic systems. PVS devices address ESD with minimal capacitance, space and cost impact. The first use of polymers for circuit protection was in resetable fuses and is well documented [12]. PVS devices represent a sister technology to the well proven polymer resetable fuses. The applications for PVS devices range from surface mount components to wafer and package level ESD protection. PVS laminate cores can be embedded in IC packages and in the board. Additionally, for system level ESD PVS ESD connector arrays require no board space and are ideally positioned to prevent high energy cable ESD from getting beyond the connector. The demonstration of PVS capability to protect GaAs is indicative of the potential for enhancing CMOS survivability at the wafer level.

Introduction of PVS devices into a variety of RF applications is made possible by using the TLP to simulate ESD pulses that correlate to device damage thresholds. The ESD specifications are constantly changing to keep pace with the electronics industry and the TLP through modification of the cable length to accommodate different pulse lengths, and the use of a very fast 200 ps rise time can simulate quite accurately the damage thresholds of actual ESD standards.

Since 1985 when the HBM specification first came out, the manufacturing environment has changed to deal with ESD issues and in doing so we have identified new needed specifications such as the MM ESD created thru handling with robots, and more recently the CDM ESD created by IC charging on conveyer belt. Now the electronic system are being routinely as handled and we are back to the human interface and the new levels of ESD created by docking and by plugging in cables. Combating the increasing variety of specifications with TLP testing is provides more damage information that ESD standard test methods. With TLP failure voltages for devices understood, it is possible to specify a PVS device with a lower voltage as a protection component to prevent ESD damage. In this mode the TLP is proving to be an incredibly useful and reliable tool.

The TLP tester and techniques described in this paper provide an engineering protocol for readily defining engineering solutions for ESD compliance with PVS devices. In our work we have modeled the IV and energy to correlate HBM, MM, CDM, IEC 6-1004-2 standards performance on the TLP with a device under test. We have developed models that correlate the performance of the TLP to these standards. With these models we can then model the PVS trigger and clamp voltages needed to protect and increase the damage threshold of the DUT. The models are in the formative stage are being put together with a combination of mathematical formulas and verification with practical testing.

VIII. Conclusion

During TLP testing the module the GSM mode was found to have a significantly lower damage threshold than the PCS/DCS mode. This was unexpected and shows the important information that is gained with TLP testing. The HBM testing had not shown a difference between the GSM and the PCS/DCS module. Incorporation of PVS devices in the module demonstrated improved ESD performance when trigger and clamp voltages were below the module damage threshold. RF testing of

the module incorporating the PVS device showed the PVS component did not interfere with RF performance and that the PVS device was comparable to a 200 fF capacitor. It is the ability of PVS devices to provide ESD protection without interfering with GHz signals that makes them and enabling technology. The PVS devices open the doorway for ESD protection of extremely ESD sensitive products such as SiGe, 60 nm CMOS, disk drive recording heads and GaAs, eliminating barriers to the constantly shrinking size and higher performance predicted by Moore's Law [13, 14, 15].

The test methods for implementing PVS components are as important as the PVS device. Without the TLP it would be very difficult to provide the PVS trigger voltage required to protect the ESD sensitive semiconductors. The TLP has demonstrated its usefulness at correlating TLP damage threshold to the PVS trigger voltage that will provide ESD protection for MM, HBM and system level ESD.

As TLP can so readily provide ESD damage threshold information, there is an emerging need for a TLP standard that can correlate to HBM, MM, CDM, IEC 6-1004-2 and the new cable ESD threats. Such a standard test protocol would greatly facilitate the introduction of reliable electronics and could do much to reverse the ESD technology roadmap trend to sacrifice reliability for enhanced performance. Such a roadmap can only lead to costly field returns. With the availability of TLP as a tool and low cost, space efficient , low capacitance PVS devices there is strong possibility for ESD damage levels to be raised over the next 5 years, not lowered. Introduction of such a TLP standard therefore could represent an immediate opportunity to increase ESD reliability of semiconductors.

Acknowledgements

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